Digitally Programmable CMOS Feedback ASIC for Network of Coupled Electromechanical Oscillators

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***Abstract*—This paper describes a programmable single-chip feedback ASIC for a network of coupled microelectromechanical systems (MEMS) referenced oscillators in the 0.4–15 MHz range. The chip contains differential low-noise amplifiers (LNAs), variable-gain amplifiers (VGAs) and programmable-gain amplifiers (PGAs) for gain control, second-order active-RC bandpass filters (BPFs) for band selection, all-pass filters (APFs) for phase shifting, an automatic level control (ALC) loop, and output buffers to drive mechanical resonators. The feedback transfer function can be fine-tuned via a three-wire serial peripheral interface (SPI) bus. A compensation path with its own PGAs, programmable attenuator, and APF enables removal of electrical feedthrough within the resonator. The chip has 5 differential input paths with independent gain control, 1-2 of which are used for local feedback (to realize oscillations) while the others accept inputs from other oscillators. The chip has been fabricated in 180 nm CMOS and consumes 4.6 mW at 1.8 V. In initial tests, it is integrated with a 2 MHz quartz resonator ($Q = 2000$) to realize an oscillator with low phase noise (-117 dBc/Hz at 1 kHz offset). Additionally, the chip's ability to synchronize oscillators is validated via a 1:1 injection locking experiment.**

***Index Terms*—Feedback ASIC, MEMS-referenced oscillators, injection locking, coupled oscillators.**

I. Introduction

Over the past decade, MEMS resonator-based oscillators have advanced toward commercialization for timing applications such as real-time clocks and wired communications standards like USB [1]–[3]. Resonant MEMS-referenced oscillators are also being used for ultrasensitive mass sensing [4], [5], inertial imaging [6], and quantum information science [7]. Recently, the synchronization of MEMS oscillators has also seen growing interest due to its applications in computing and information processing [8], [9]. Arrays of coupled oscillators can implement Ising machines for solving nondeterministic polynomial-time hard (NP-hard) problems, which are computationally challenging to solve in digital computers. Finding the best solution reduces to locating the Ising model's ground state, which is accomplished using networks of coupled artificial spins. Fig. 1 shows an overview of oscillator-based Ising machines (1D and 2D coupled oscillator networks) which typically use subharmonic injection locking as the annealing mechanism [10] to solve NP-hard problems, such as the weighted Max-Cut problem [11]. Though significant attention has been paid to LC, memristor, and ring oscillator-based Ising machines [12]–[14], miniaturized low-power versions using arrays of resonant MEMS-referenced oscillators have not yet been experimentally demonstrated.

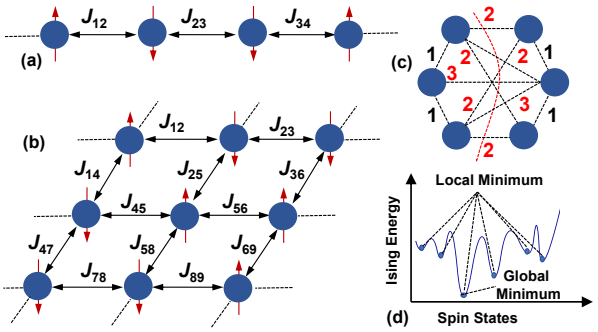

Fig. 1. Overview of oscillator-based Ising machines for solving NP-hard problems: (a) 1D network, and (b) 2D network. (c) Solving a 6-node Max-Cut problem using an Ising model, and (d) its energy landscape.

In this paper, we describe a CMOS feedback ASIC for interfacing with coupled self-sustaining MEMS-referenced oscillators in the 0.4-15 MHz range, in order to enable building blocks for future MEMS-enabled Ising machines. As shown in Fig. 2, the chip contains 5 input paths (LNA and VGA) with programmable gains, w_i, and a signal combiner. Up to 4 of these paths can be driven by external inputs (e.g., other oscillators) to realize 1D/2D networks of coupled oscillators. The summed signal is further processed by the on-chip BPFs, APFs, and PGAs before driving (1) up to 2 MEMS resonators (thus realizing local feedback loops to generate oscillations), and (2) other oscillators in the network.

II. Feedback ASIC Design

Fig. 3 shows a more detailed block diagram of the chip, which includes LNAs, VGAs, PGAs, APFs, differential output buffers, and an ALC loop based on an envelope detector (ED). There are two output signals (main, v_{OUT}, and compensation, v_{CMP}) with adjustable relative gain and phase shift. All chip parameters (e.g., BPF gain, center frequency, and Q; gains of PGA, VGA and LNA; and APF phase shifts) can be programmed via a standard 3-wire SPI port.

A. LNA and VGA Design

The chip improves upon earlier programmable CMOS feedback ASICs (i.e., sustaining amplifiers) [15]–[17] by including five independently-programmable input paths (Fig. 2). The LNA in each path also has improved performance compared

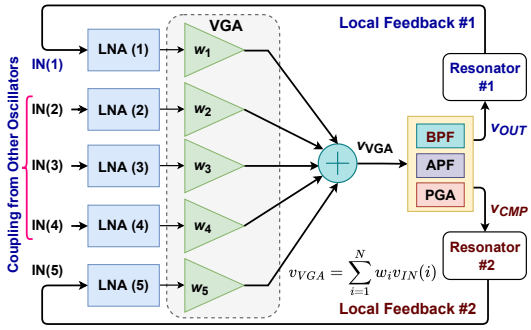

Fig. 2. Coupling mechanism used by the ASIC to build oscillator networks.

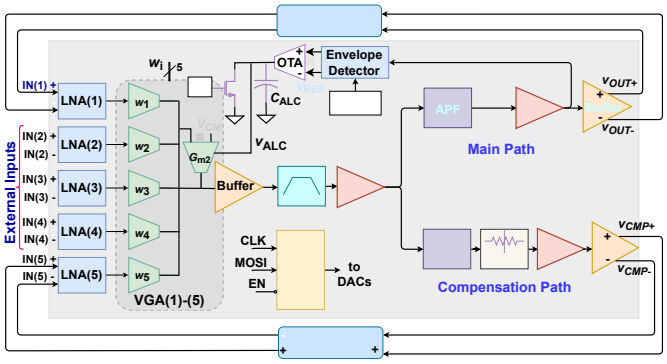

Fig. 3. Architecture of the feedback ASIC for interfacing with generic MEMS resonators. Attn.: attenuator; OTA: operational transconductance amplifier.

to previous work. Fig. 4 shows the schematic of each LNA. The design is a fully-differential common-source amplifier with capacitive feedback to set the voltage gain. Current reuse (via an active PMOS load) is used to (1) reduce input-referred noise, and (2) keep the output DC operating point independent of bias current I_{LNA}. To increase open-loop gain, the input pair and the load are both cascoded, with their DC operating points set via active MOS resistors controlled by the auxiliary bias current I_{B1}. The nominal closed-loop gain is $A_0 \approx -(g_{\mathrm{mp}}/g_{\mathrm{mn}})(1+C_{\mathrm{IN}}/C_{\mathrm{F}})-C_{\mathrm{IN}}/C_{\mathrm{F}} = 26$ dB where g_{mn} and g_{mp} are the transconductances of the NMOS input pair and active PMOS load, respectively. The switches $\mathrm{SW}_{1,2}$ increase C_{F} by $2\times$ to reduce A_0 by 6 dB if needed, thus increasing the overall dynamic range (DR). The typical input-referred noise PSD is 3.8 nV/Hz$^{1/2}$ at $I_{\mathrm{LNA}} = 20$ μA.

The chip integrates five differential input channels (LNA and VGA) to enable the design of 1D/2D coupled oscillator networks. The VGA is realized by 1) converting the LNA outputs to current using OTAs (G_{m1}), 2) summing the OTA outputs in current-mode, and 3) converting the sum to voltage using a load OTA (G_{m2}), as shown in Fig. 3. Each channel includes both 5-bit digital gain control and sign control for G_{m1}, such that the output voltage can be written as

$$v_{OUT} = \frac{1}{G_{\mathrm{m2}}} \sum_{i=1}^{5} s_i G_{\mathrm{LNA},i} G_{\mathrm{m1},i} v_{IN,i}, \qquad (1)$$

where $s_i \in \{+1, -1\}$ is the sign and $G_{\mathrm{m1},i}$ is programmable. The load OTA's transconductance is given by $G_{\mathrm{m2}} = (I_{\mathrm{B2}} + I_{\mathrm{ALC}})/V_{\mathrm{L2}}$ where I_{B2} and V_{L2} are the nominal

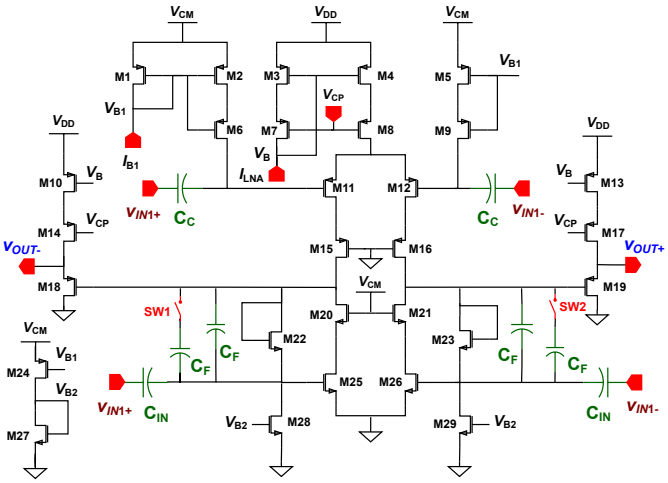

Fig. 4. Schematic of a single fully-differential LNA.

bias current and linear range, respectively, and I_{ALC} is a feedback current set by an automatic level control (ALC) loop.

The input-referred DR of the chip is increased by enhancing the linear range of the OTAs in the VGA. Resistive source degeneration is used for this purpose, with the tail current source split to avoid degradation of input common-mode range [18]. The typical linear range (at $I_{\mathrm{B}} = 5$ μA) is 350 mV and increases further with I_{B}. The value of G_{m} for a given I_{B} can be varied via a 4-bit current DAC within the OTA that provides programmable current gain between the input and output stages. At the minimum gain setting, the input-referred linear range for each input channel exceeds 80 mVpk (-12 dBm), which is $20\times$ larger than earlier designs [17].

B. BPF Design

The BPF consists of two cascaded Tow-Thomas biquads, resulting in a fourth-order response. The ideal transfer function of each biquad can be written as

$$H_{\mathrm{BPF}}(s) = G\left(\frac{s\tau/Q}{s^2\tau^2 + s\tau/Q + 1}\right). \qquad (2)$$

Here, $Q = R_{\mathrm{d}}/R$, $\omega_0 = 1/\tau = 1/(RC)$, and $G = R_{\mathrm{d}}/R_{\mathrm{g}} = Q(R/R_{\mathrm{g}})$. The center frequency, gain and Q can be tuned using R_{g} , R_{d} and C, which are controlled by 5-bit resistive and 4-bit capacitive DACs, respectively.

The Tow-Thomas biquad topology has a well-known problem: finite op-amp bandwidth ω_1 increases the effective Q to $Q_{\mathrm{a}} \approx Q/(1 - 4\omega_0 Q/\omega_1)$, which reduces Q-tuning range and can lead to instability [19]. As shown in Fig. 5, a feed-forward compensation path (in red) was added around the second op-amp ($U2$) to reduce this effect. The effective Q becomes $Q_{\mathrm{a}} \approx Q/(1 - 2\omega_0 Q/\omega_1)$, so the problem is reduced by $2\times$.

C. Design of Other Blocks

The chip contains PGAs and programmable APFs to adjust the feedback gain and phase, respectively, for realizing oscillators. Both blocks use conventional designs that combine op-amps with capacitive and/or resistive DACs for tuning, and are

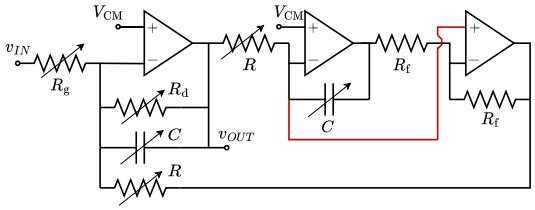

Fig. 5. Schematic of the modified Tow-Thomas biquad within the BPF.

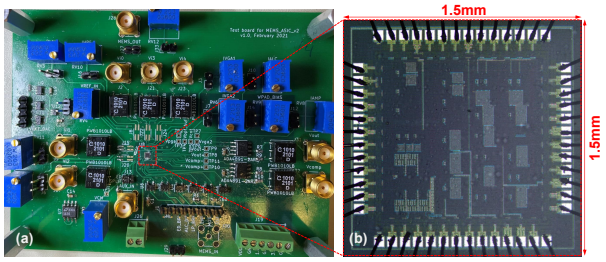

Fig. 6. (a) Test PCB containing the wirebonded ASIC, and (b) die micrograph of the feedback ASIC implemented in UMC 180 nm CMOS.

not described here. The main signal path contains three PGAs and two APFs, each of which can provide a gain range of 0-24 dB and a phase shift range of $0-120°$, respectively. Thus, the feedback TF can be set over a broad range, making the chip suitable for use with a variety of MEMS/NEMS resonators.

The chip has two signal paths for driving resonators, with outputs denoted by v_{OUT} and v_{CMP}. The latter has its own PGAs, attenuator, and APF, so the two paths can be controlled independently. The op-amps in the differential output buffers contain small series resistors to ensure stability with large capacitive loads. In-pad OTA-based voltage buffers allow monitoring of signals at various stages in the sustaining amplifier.

III. Experimental Results

A. ASIC Electrical Test Results

The ASIC was designed and taped-out in 180 nm standard CMOS technology. Fig. 6 shows the ASIC die (1.5 mm $\times$ 1.5 mm) along with its test PCB, which can also be used to mount the MEMS die. The nominal supply voltage and power consumption of the chip are 1.8 V and 4.6 mW, respectively.

Individual input channels (LNA$_i$ and VGA$_i$, $i \in \{1-5\}$) were tested by programming the VGA gains over SPI. Each channel was measured in both high- and low-gain modes at 1 MHz; the resulting gain ranges were found to be 5-27 dB and 0.5-21 dB, respectively, in good agreement with simulations. Fig. 7 summarizes the data for channels #1, #2, and #4.

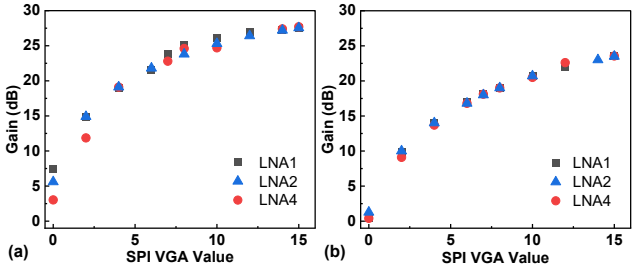

Fig. 7. LNA-VGA gain calibration: (a) High-gain mode (b) Low-gain mode.

Weighted summation of input signals was tested by feeding channels #1 and #2 with sinusoidal inputs at 1 MHz (2 mV amplitude) and 2.2 MHz (2.5 mV amplitude), respectively. The gain of channel #1 was kept fixed at 23.5 dB, while that of channel #4 was varied (both in magnitude and sign). The sum/difference signal was observed using an oscilloscope and converted to the frequency domain. Fig. 8 shows the output spectra, which confirm that the signed weights of the channels can be individually programmed. Thus, the chip can realize programmable inter-oscillator coupling strengths for implementing a variety of Ising machines.

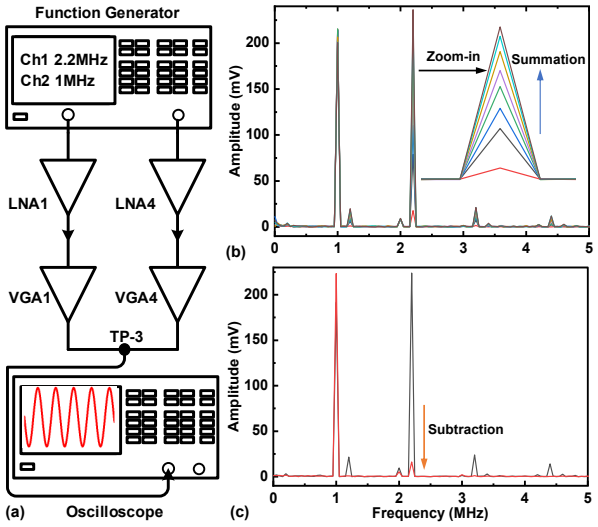

Fig. 8. Weighted summation of channels #1 and #4. (a) Measurement setup. (b) Output spectrum for varying channel #4 gain. (c) Subtraction of two inputs by flipping the phase of VGA4. The red line shows the data after subtraction.

The BPF center frequency, ω_0, and gain, G, were tuned via the values of both R and C DACs. During calibration, we (1) fixed $R = 2$, $R_d = 15$, and $R_g = 15$ and tuned C to program ω_0; and (2) fixed $\omega_0 = 1.06$ MHz, $R_g = 1$, $R = 12$, and $C = 15$ and tuned R_d to program G. Fig. 9 shows the calibration curves for ω_0 and G, which agree with simulations.

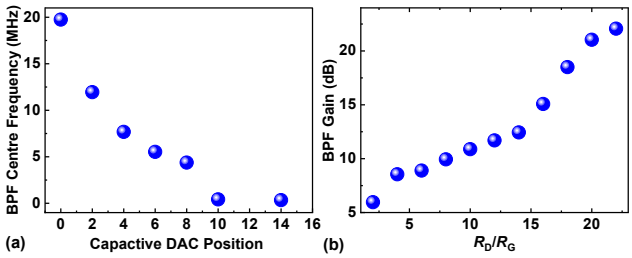

Fig. 9. BPF test results: (a) Center frequency calibration, (b) Gain calibration.

B. Quartz Crystal Oscillator Demonstration using the ASIC

We tested the ASIC using a 2 MHz quartz crystal resonator ($Q \approx 2000$) with a peak transmission of -15 dB and peak to background ratio of 8 dB. Fig. 10 shows the measurement setup and transmission, $|S_{21}|$, of the chosen quartz resonator. Next, the PGA gain and APF phase shift were adjusted to

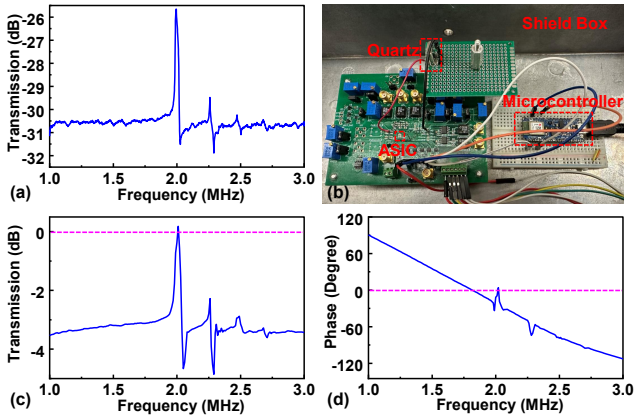

Fig. 10. Quartz crystal resonator open-loop characterization results: (a) Transmission, $|S_{21}|$. (b) Test circuit setup. Open-loop measurement with the resonator and ASIC: (c) gain, and (d) phase response.

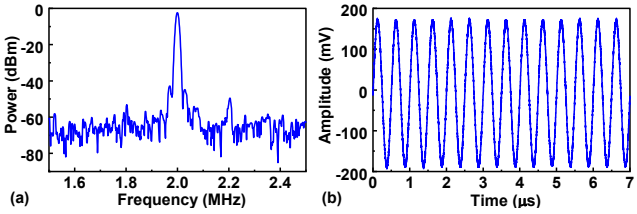

Fig. 11. Closed-loop response. (a) Frequency-domain output spectrum of the feedbak oscillator. (b) Time-domain output waveform of the oscillator.

obtain an open-loop gain and phase shift slightly > 0 dB and 0° at 2 MHz, respectively, as shown in Figs. 10(c)-(d).

The feedback loop was then closed to obtain self-sustained oscillations. The output was measured in both the frequency-domain and time-domain by using a spectrum analyzer and oscilloscope, respectively. Typical measurement results exhibit near-sinusoidal oscillations, as shown in Fig. 11.

Oscillator performance was further studied by measuring the phase noise spectrum, as shown in Fig. 12. The figure reveals a $1/f^3$ region at low offset frequencies (10-470 Hz) that is assumed to be dominated by electronic flicker noise mechanisms. The spectrum flattens out at larger offsets, which indicates that amplitude noise is dominant in this region. The measured phase noise was empirically fitted to the Leeson model [20], [21], yielding an equivalent noise factor of $F_{\rm n} = 11$ and a $1/f^3$ corner frequency of 470 Hz. The phase noise at 1 kHz offset (which is a common figure of merit for oscillators) is approximately -100 dBc/Hz. The unwanted tones observed at frequency offsets between 10^4-10^6 Hz may be due to coupling of external noise into the DC power supply.

To improve the oscillator performance, the quartz crystal resonator was soldered on a small board and stacked on the PCB containing the ASIC as shown in Fig. 10(b). The stacked boards were placed in a metal box to minimize external pickup. The open- and closed-loop responses were largely unchanged. However, the measured phase noise shows significant improvement (Fig. 12). At 1 kHz offset, we now obtain -117 dBc/Hz, which is $\sim$17 dB lower than before. By fitting the Leeson model, we obtain an excellent equivalent noise factor of $F_{\rm n} = 4$ (about $2.75\times$ lower than before) and a

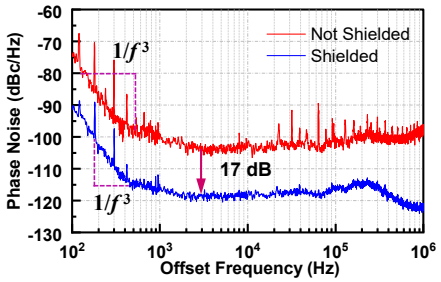

Fig. 12. Phase noise performance of the quartz oscillator. The shielded configuration results in $\sim$17 dB reduction in phase noise.

$1/f^3$ corner frequency of 570 Hz. Shielding also suppresses unwanted spikes in the phase noise PSD, as visible in Fig. 12.

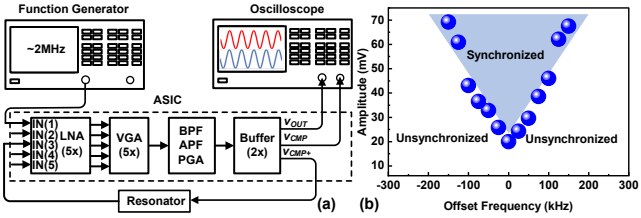

Fig. 13. Results of an 1:1 injection locking experiment. (a) Measurement setup. (b) Arnold tongue diagram showing the synchronized region.

C. Injection Locking of the Oscillator

We performed an 1:1 injection locking experiment using the quartz-referenced oscillator to verify the chip's capability to realize coupled oscillators. As the first step, instead of coupling to another quartz or MEMS oscillator, a function generator was used to provide an injection locking signal at a frequency, f_1, near the quartz resonance frequency, f_0. This injection locking signal acts as a 'synchronizing' perturbation, i.e., establishes a weak dynamic coupling between the oscillator and an external reference [22]. The offset frequency, $\Delta f = (f_1 - f_0)$, was varied from -300 to 300 kHz with the f_1 signal amplitude increased from 5-70 mV at each frequency. Fig. 13 shows the measurement results, which clearly reveal the expected 'Arnold tongue' shape of the injection-locked state around $\Delta f = 0$. The width of this region is much larger than the bandwidth of the open-loop resonator (about 1 kHz), which suggests that the injected signal is primarily perturbing the transfer function of the ASIC.

IV. Conclusions

We have demonstrated a programmable CMOS feedback ASIC that can be used to facilitate coupled self-sustaining mechanical oscillators. We have electrically characterized the chip and built a low-phase-noise quartz crystal resonator-referenced oscillator as an initial test. We have also demonstrated 1:1 injection locking to external reference, thus validating the chip's ability to implement inter-oscillator coupling. Future work will focus on implementing MEMS-referenced oscillators and their networks as miniaturized and energy-efficient Ising machines for solving NP-hard problems.

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REFERENCES

[1] J. van Beek and R. Puers, "A review of MEMS oscillators for frequency reference and timing applications," *Journal of Micromechanics and Microengineering*, vol. 22, no. 1, p. 013001, 2011.

[2] M.-H. Li, C.-Y. Chen, C.-S. Li, C.-H. Chin, and S.-S. Li, "A monolithic CMOS-MEMS oscillator based on an ultra-low-power ovenized micromechanical resonator," *Journal of Microelectromechanical Systems*, vol. 24, no. 2, pp. 360–372, 2014.

[3] C.-S. Liu, R. Tabrizian, and F. Ayazi, "A $\pm$0.3 ppm oven-controlled MEMS oscillator using structural resistance-based temperature sensing," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 65, no. 8, pp. 1492–1499, 2018.

[4] C.-H. Weng, G. Pillai, and S.-S. Li, "A thin-film piezoelectric-on-silicon MEMS oscillator for mass sensing applications," *IEEE Sensors Journal*, vol. 20, no. 13, pp. 7001–7009, 2020.

[5] M. Chellasivalingam, A. T. Zielinski, T. S. Whitney, A. M. Boies, and A. A. Seshia, "Towards portable MEMS oscillators for sensing nanoparticles," *Sensors*, vol. 22, no. 15, p. 5485, 2022.

[6] M. S. Hanay, S. I. Kelber, C. D. O'Connell, P. Mulvaney, J. E. Sader, and M. L. Roukes, "Inertial imaging with nanomechanical systems," *Nature Nanotechnology*, vol. 10, no. 4, pp. 339–344, 2015.

[7] A. D. O'Connell, M. Hofheinz, M. Ansmann, R. C. Bialczak, M. Lenander, E. Lucero, M. Neeley, D. Sank, H. Wang, M. Weides, J. Wenner, J. M. Martinis, and A. N. Cleland, "Quantum ground state and single-phonon control of a mechanical resonator," *Nature Nanotechnology*, vol. 464, no. 7289, pp. 697–703, 2010.

[8] F. Hoppensteadt and E. Izhikevich, "Synchronization of MEMS resonators and mechanical neurocomputing," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 2, pp. 133–138, 2001.

[9] I. Mahboob and H. Yamaguchi, "Bit storage and bit flip operations in an electromechanical oscillator," *Nature Nanotechnology*, vol. 3, no. 5, pp. 275–279, 2008.

[10] A. Neogy and J. Roychowdhury, "Analysis and design of sub-harmonically injection locked oscillators," in *2012 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2012, pp. 1209–1214.

[11] J. Chou, S. Bramhavar, S. Ghosh, and W. Herzog, "Analog coupled oscillator based weighted Ising machine," *Scientific Reports*, vol. 9, no. 1, p. 1786, 2019.

[12] T. Wang, L. Wu, P. Nobel, and J. Roychowdhury, "Solving combinatorial optimisation problems using oscillator based Ising machines," *Natural Computing*, vol. 20, no. 2, pp. 287–306, 2021.

[13] S. Dutta, A. Khanna, J. Gomez, K. Ni, Z. Toroczkai, and S. Datta, "Experimental demonstration of phase transition nano-oscillator based Ising machine," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, pp. 37.8.1–37.8.4.

[14] I. Ahmed, P.-W. Chiu, W. Moy, and C. H. Kim, "A probabilistic compute fabric based on coupled ring oscillators for solving combinatorial optimization problems," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 9, pp. 2870–2880, 2021.

[15] M. S. Islam, R. Wei, J. Lee, Y. Xie, S. Mandal, and P. X.-L. Feng, "A temperature-compensated single-crystal silicon-on-insulator (SOI) MEMS oscillator with a CMOS amplifier chip," *Micromachines*, vol. 9, no. 11, p. 559, 2018.

[16] M. S. Islam, S. K. Singh, J. Lee, Y. Xie, C. A. Zorman, P. X.-L. Feng, and S. Mandal, "A programmable sustaining amplifier for flexible multimode MEMS-referenced oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 4, pp. 1405–1418, 2018.

[17] M. S. Islam, S. K. Singh, G. Xereas, V. P. Chodavarapu, and S. Mandal, "A digitally programmable CMOS feedback ASIC for highly stable MEMS-referenced oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 11, pp. 4158–4171, 2019.

[18] A. Murugesan, "An N-port quadrature ADC using 2-D space-time delta-sigma noise-shaping for N-element antenna array receivers," M.S.Thesis, 2021, University of Florida.

[19] A. M. Soliman, "History and progress of the Tow–Thomas bi-quadratic filter part I: Generation and op amp realizations," *Journal of Circuits, Systems, and Computers*, vol. 17, no. 01, pp. 33–54, 2008.

[20] X. L. Feng, C. J. White, A. Hajimiri, and M. L. Roukes, "A self-sustaining ultrahigh-frequency nanoelectromechanical oscillator," *Nature Nanotechnology*, vol. 3, no. 6, pp. 342–346, 2008.

[21] D. B. Leeson, "Oscillator phase noise: A 50-year review," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 8, pp. 1208–1225, 2016.

[22] A. Pikovsky, M. Rosenblum, and J. Kurths, *Synchronization: A universal concept in nonlinear sciences*, ser. Cambridge nonlinear science series. Cambridge, England: Cambridge University Press, Oct. 2001.