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Traditional Packaging Technology

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Pin Through Hole

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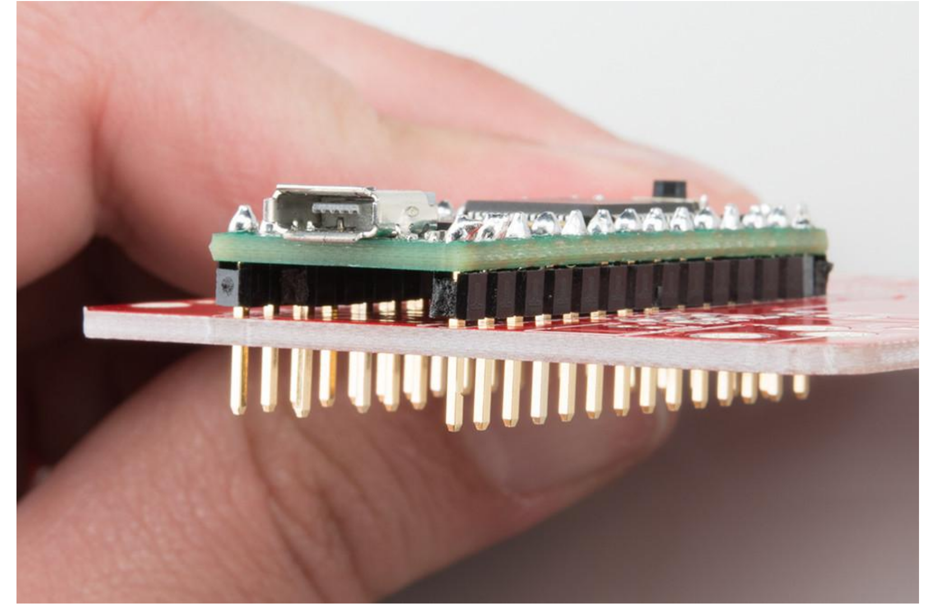
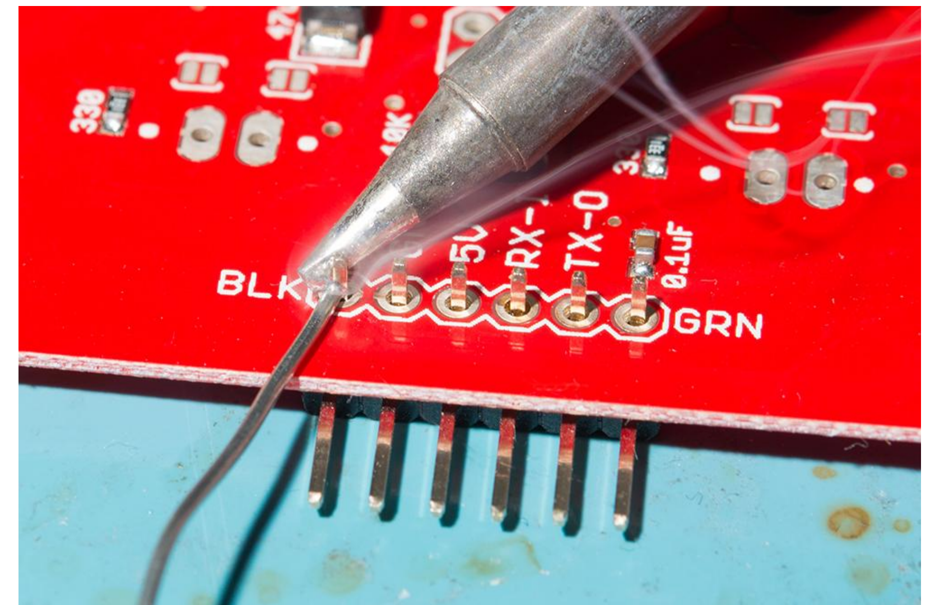
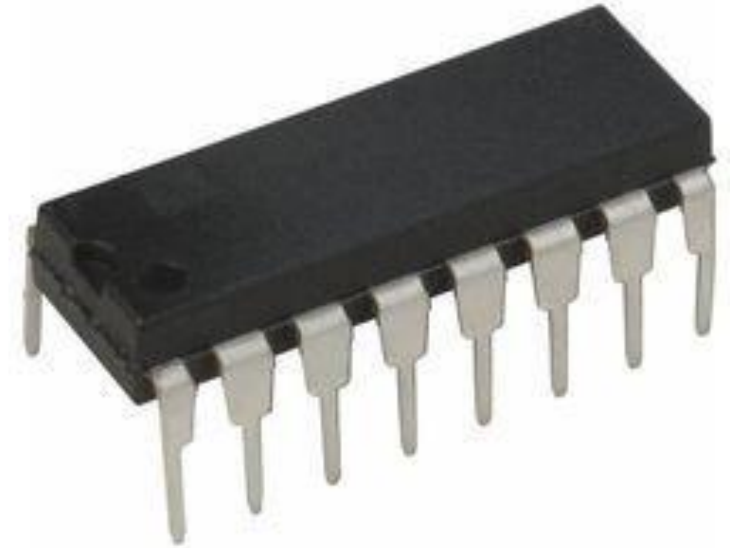
- Pin inserted into socket or soldered through hole of PCB
- DIP – Dual Inline Packaging
- SIP – Single Inline Packaging
- CDIP – Ceramic DIP





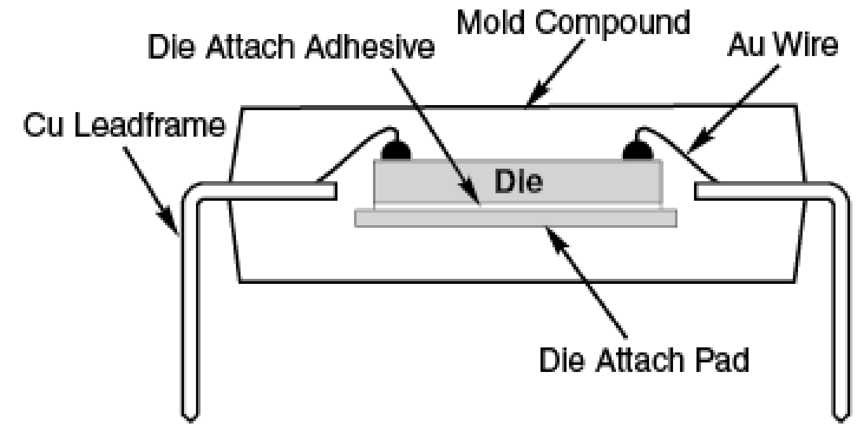
DIP – Dual Inline Package

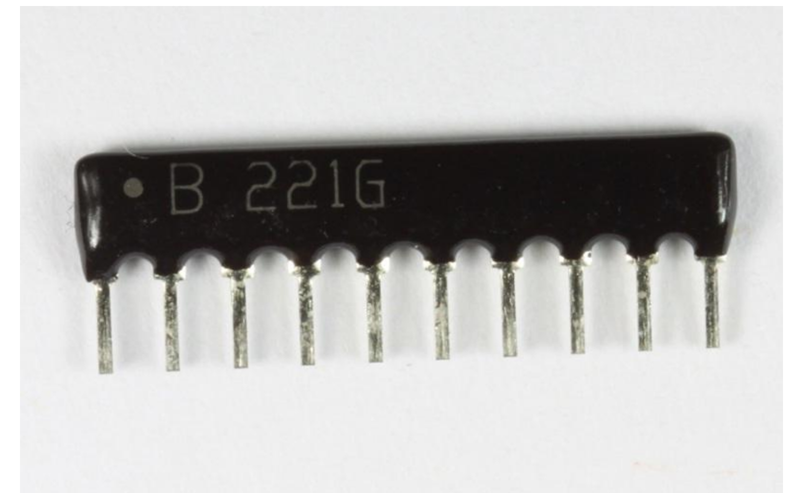
- Invented in 1964 at Fairchild – 14 pins.
- Easy automatic assembly
- Pin count: 4 – 64
- Structure of the chip limits maximum number of pins
- Package is much larger than die
- Notch helps assembly



DIP + SIP

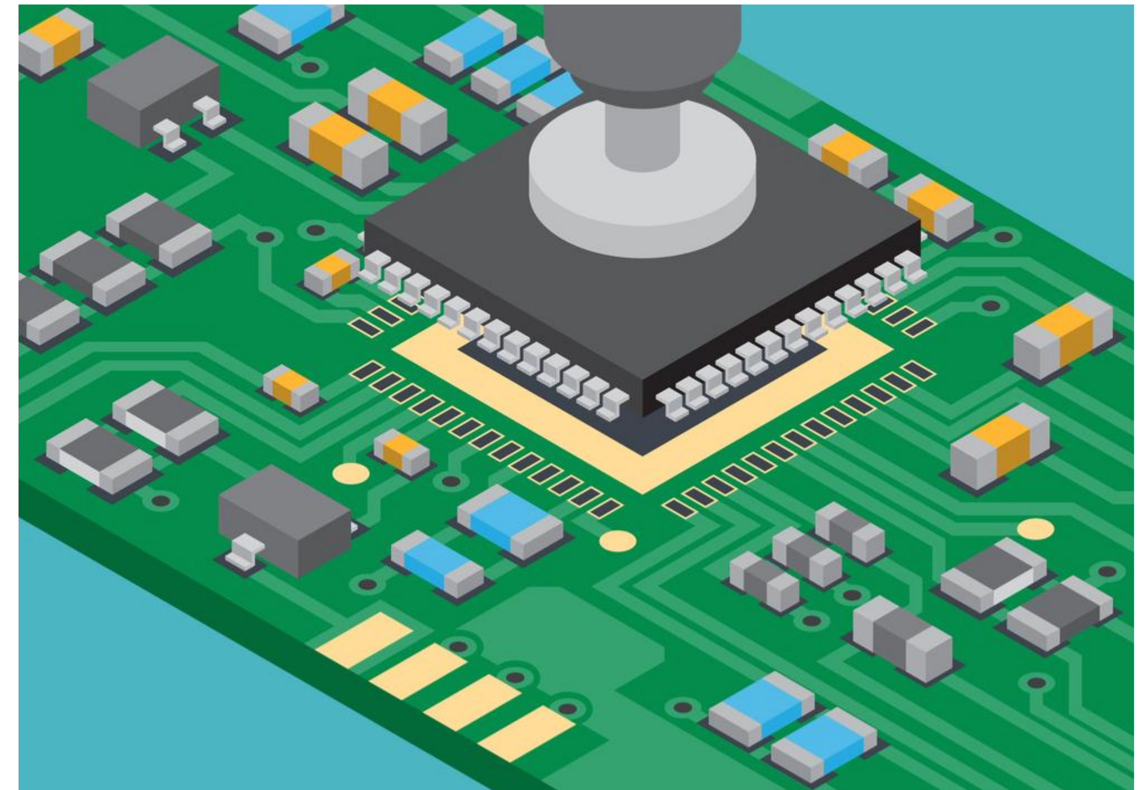
- Plastic or ceramic mold
- Leads wire bonded to silicon die.
- Fell off with introduction of SMT
- SIP
  - Similar to DIP
  - Only one line of leads with common pin
  - Mainly used for memory modules
  - Pin Count: up to 24 pins





Surface Mount Technology

- Solders directly on top of board
- Smaller than Pin Through Hole
- Easier and faster automated assembly
- QFP – Quad Flat Package
- PGA – Pin Grid Array
- BGA – Ball Grid Array



QFP – Quad Flat Package

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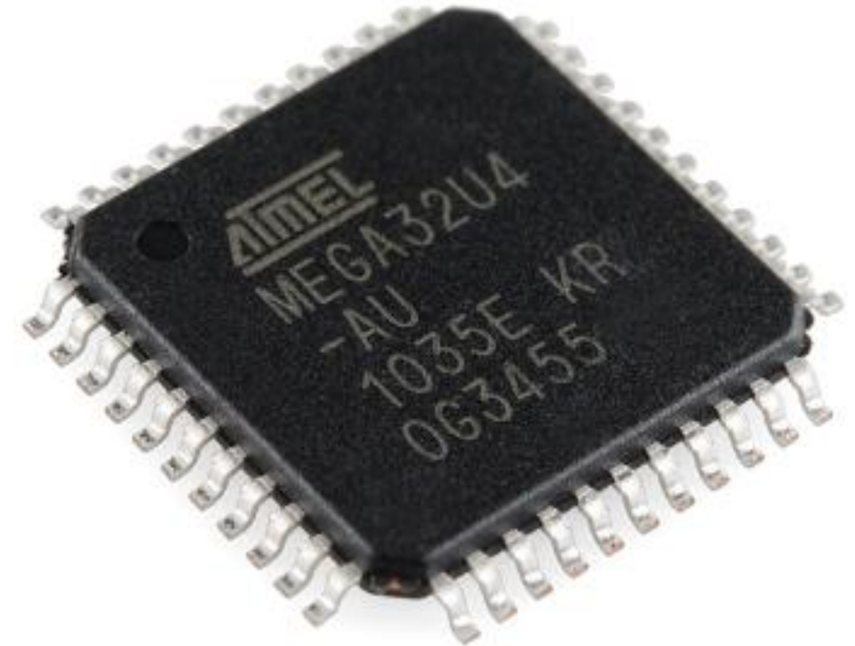
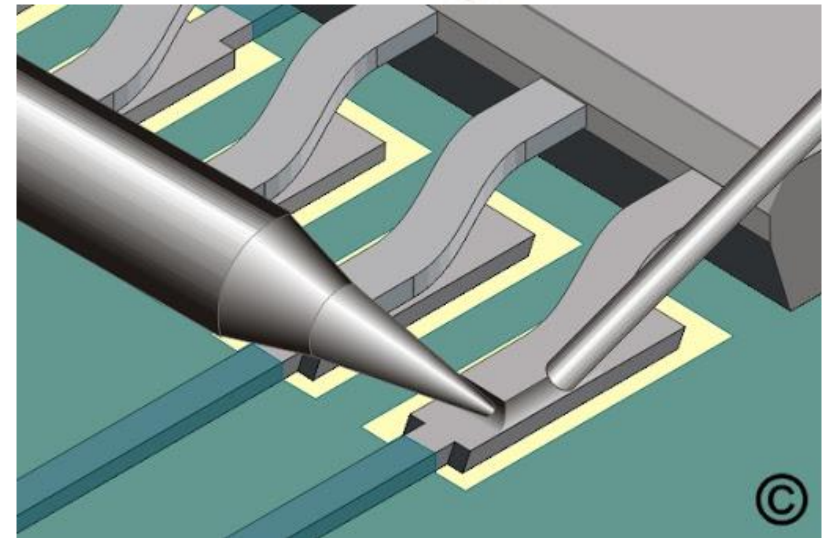
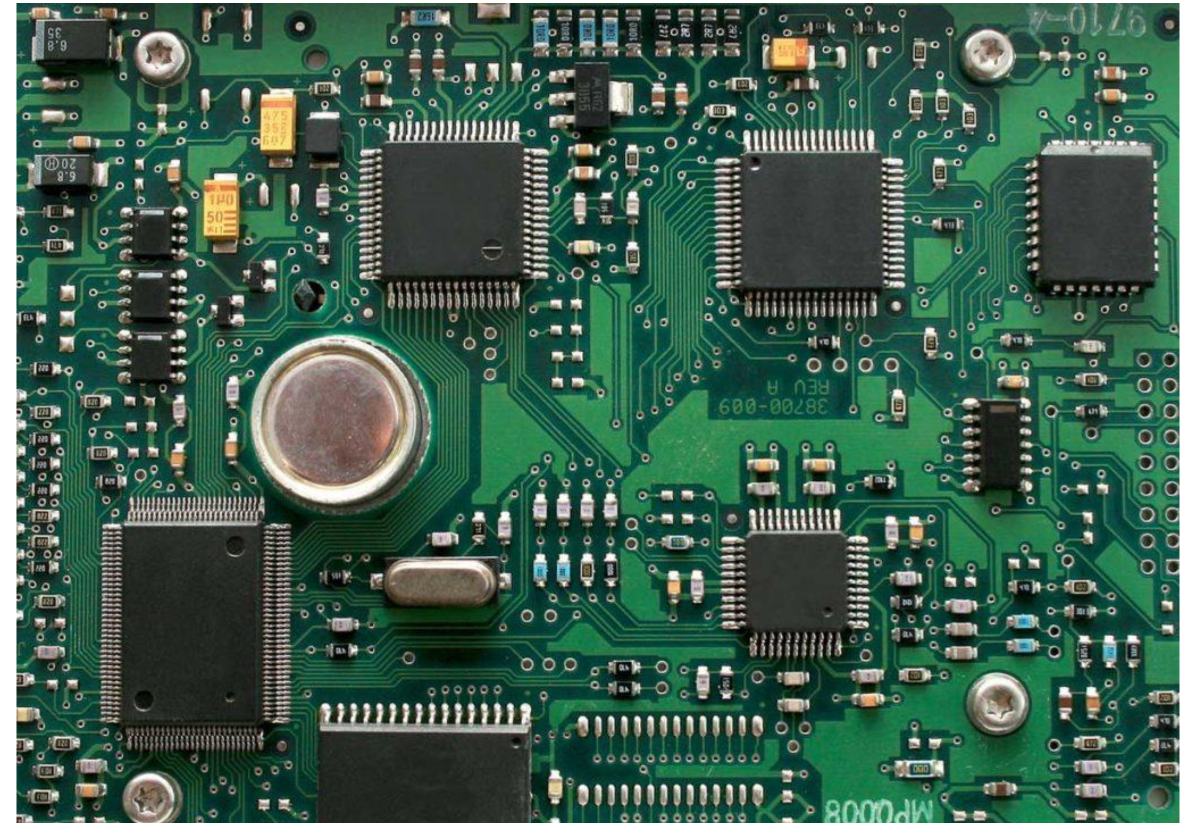
- Developed in the 60s, first used commercially in the 80s
- Much higher number of Pins
  - Pin Count: 32 – 304 pins
- Gull wing shaped leads on four sides
- Pins may suffer damage by handling.
- PCB Track density issues





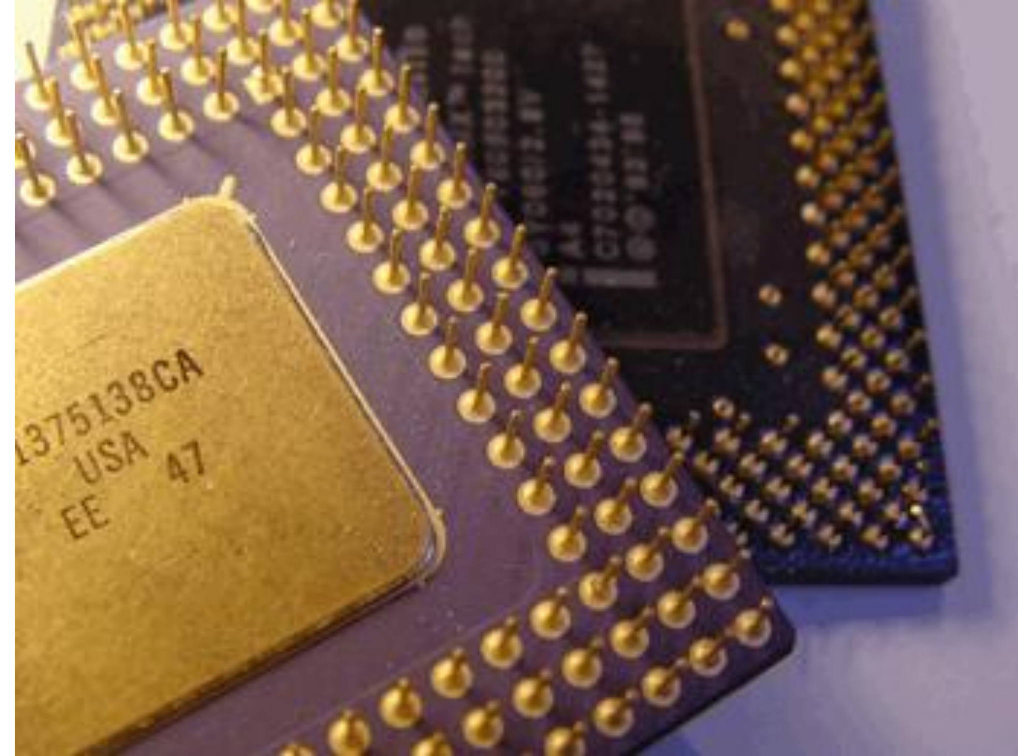
QFP – Quad Flat Package

- Common Types:
  - PQFP – Plastic QFP
  - CQFP – Ceramic QFP
  - FQFP – Fine Pitched QFP
  - HQFP – Heat sinked QFP
  - LQFP – Low profile QFP
- Widely used for ICs today
- Fell off for higher density PGA and BGA



PGA – Pin Grid Array

- PPGA developed by Intel in 1993
- Needed for transition from 16 to 32 bits
- Pins on surface of the chip, arranged in a grid array.
- Number of pins outnumbers any previous technologies
- More fragile and unreliable
- Fell off because it's fragile and BGA took over

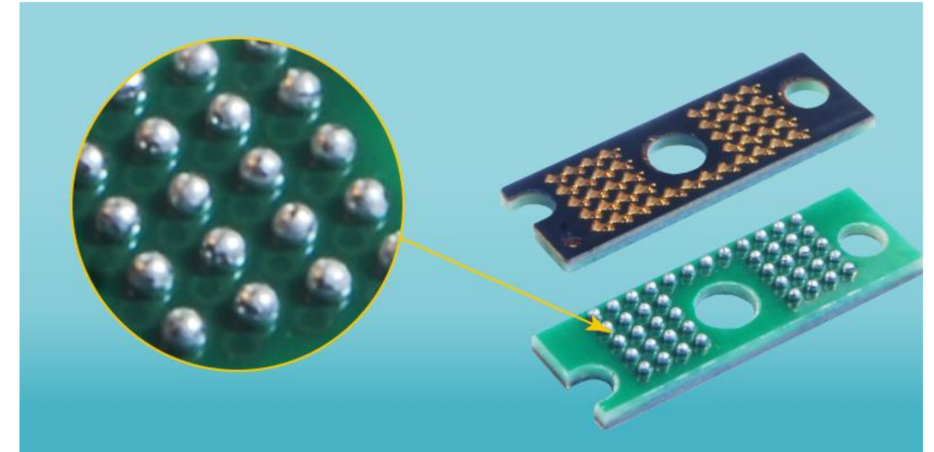


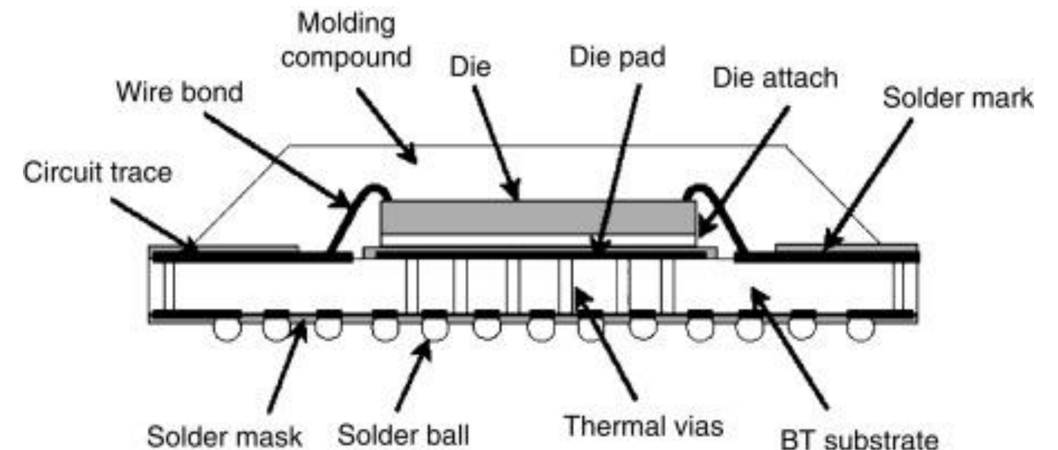
PGA – Pin Grid Array

- Types:
  - Plastic — PGA in plastic packaging
  - Ceramic — PGA in ceramic packaging
  - Flip-chip — Die facing downwards on top of the substrate
  - Staggered — Pin layout staggered for tight compression
  - Organic — Die attached to an organic plate
- Usually used for computer chips
  - Intel's Pentium III microprocessor

BGA – Ball Grid Array

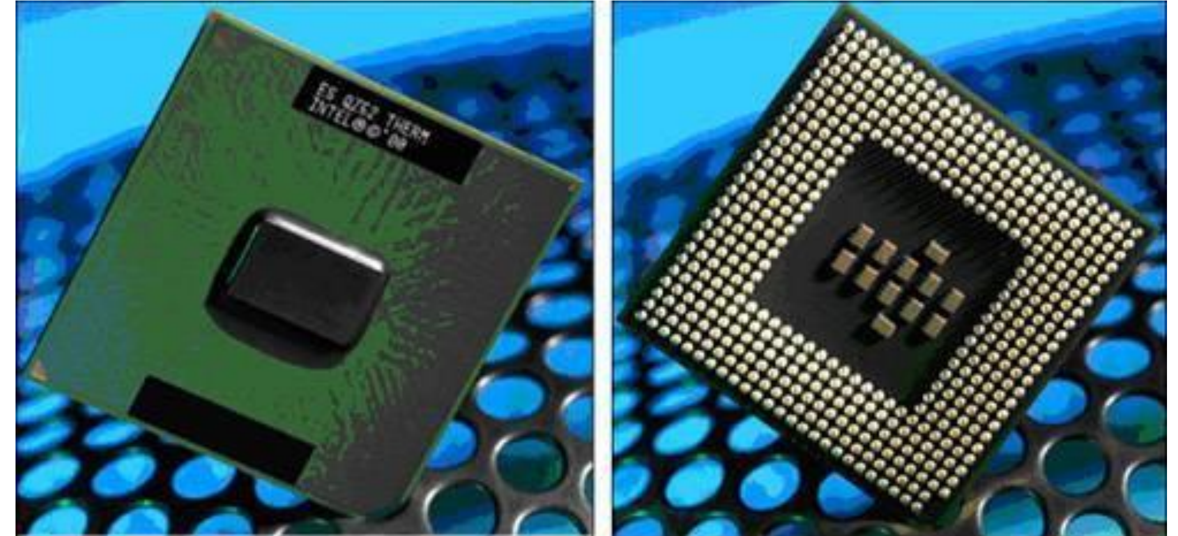
- Motorola and Citizen jointly developed the plastic BGA in 1989
- Another solution to the I/O limitations of QFPs
- Uses solder balls instead of pins
- Higher performance, higher speeds, more resilient.
- Less reliability in extreme conditions, difficult inspection.
- Widely used today

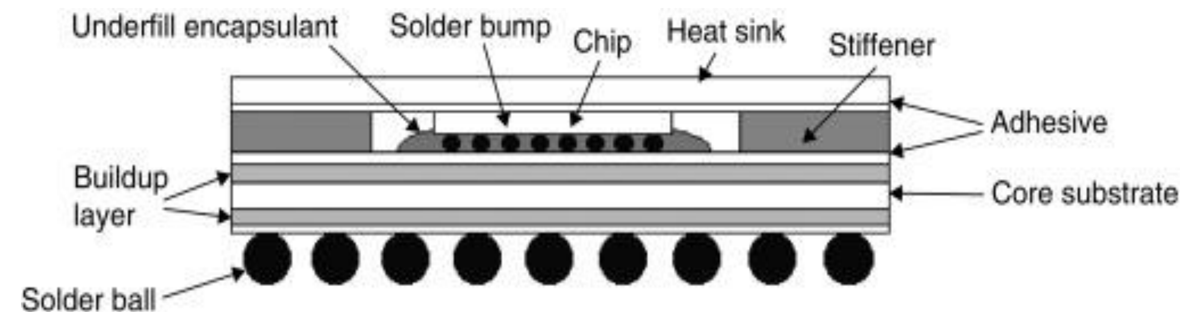




BGA – Ball Grid Array

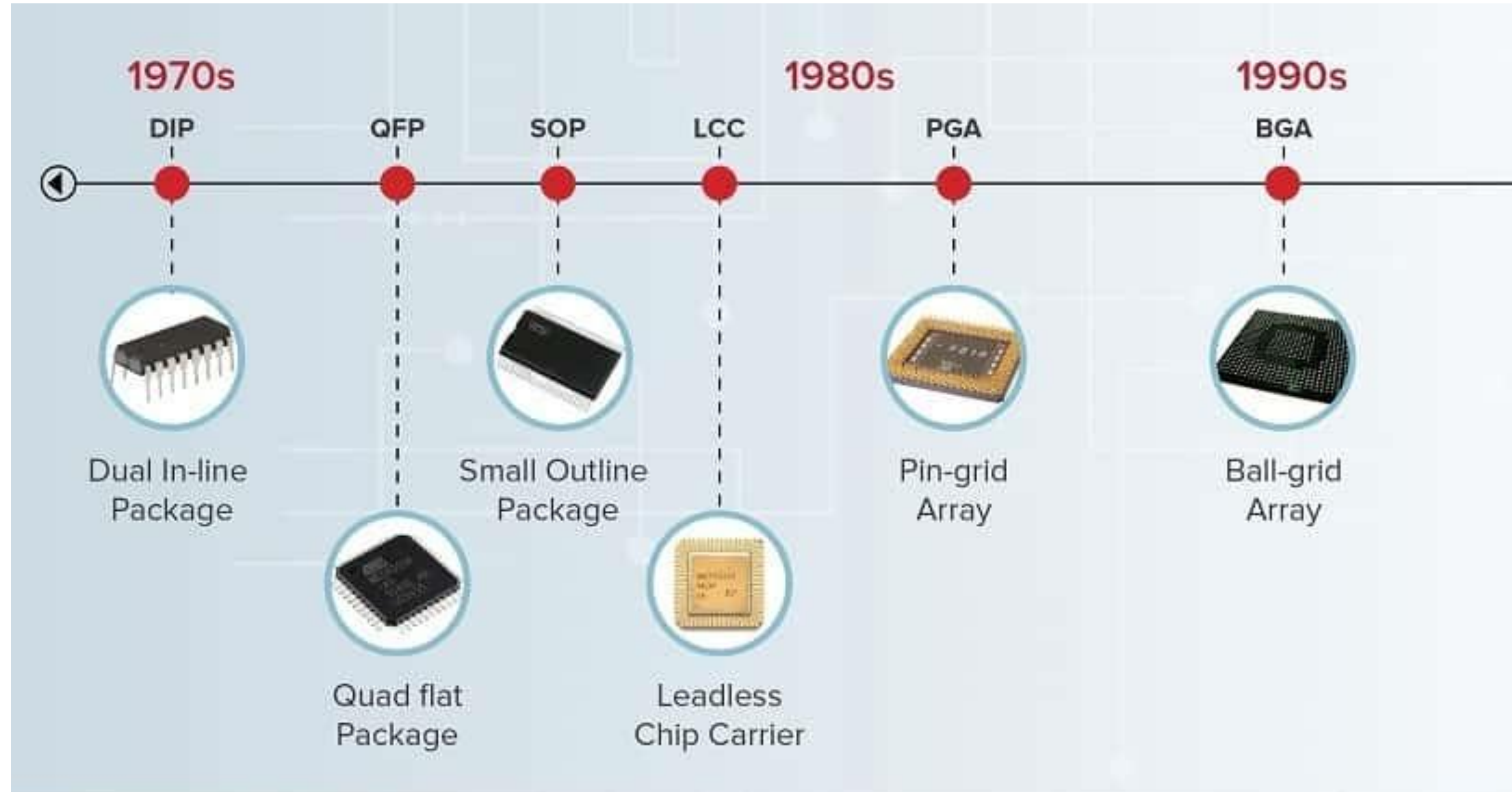
- Common types:
  - PBGA – Plastic BGA
  - CBGA – Ceramic BGA
  - TBGA – Tape or Tab BGA
  - SBGA – Super BGA
- Used for many purposes
  - “Micro-FCBGA” – Intel’s mounting method for mobile processors, introduced with the Coppermine Mobile Celeron





Summary

- ❖ Pin Through Hole
  - ➢ DIP
  - ➢ SIP
- ❖ Surface Mount technology
  - ➢ QFP
  - ➢ PGA
  - ➢ BGA



Introduction of IC Packaging

Foundries

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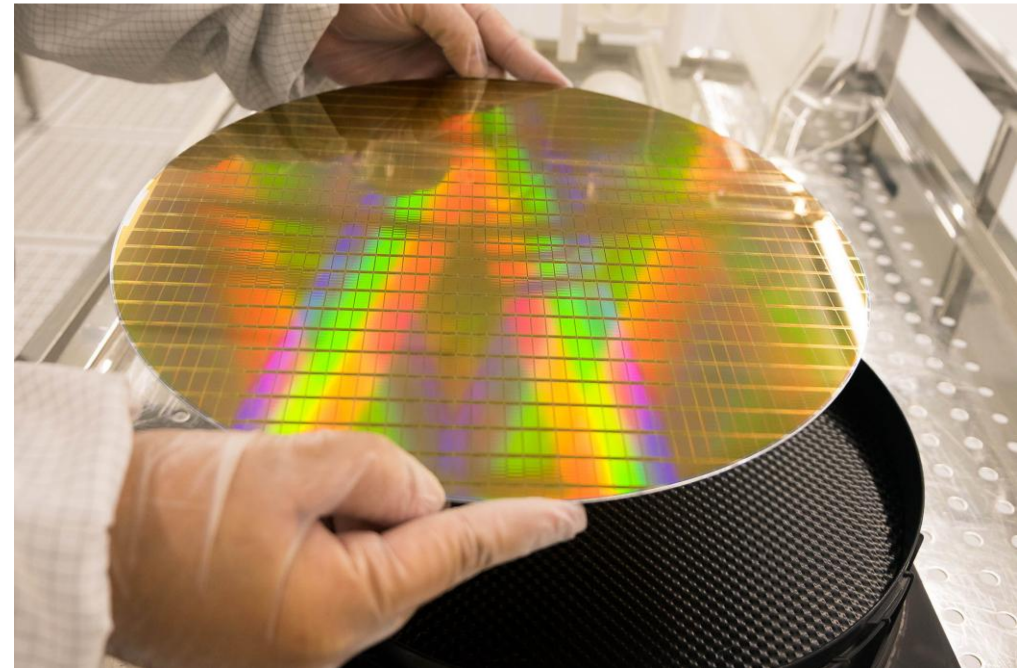
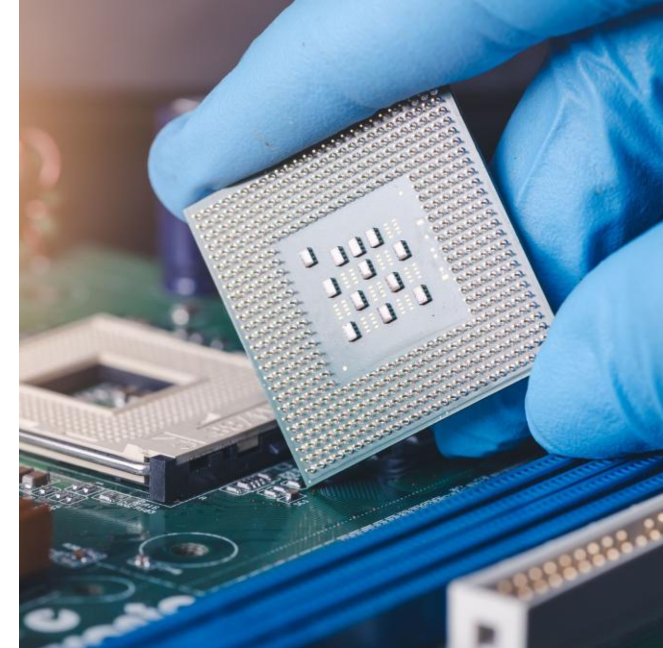
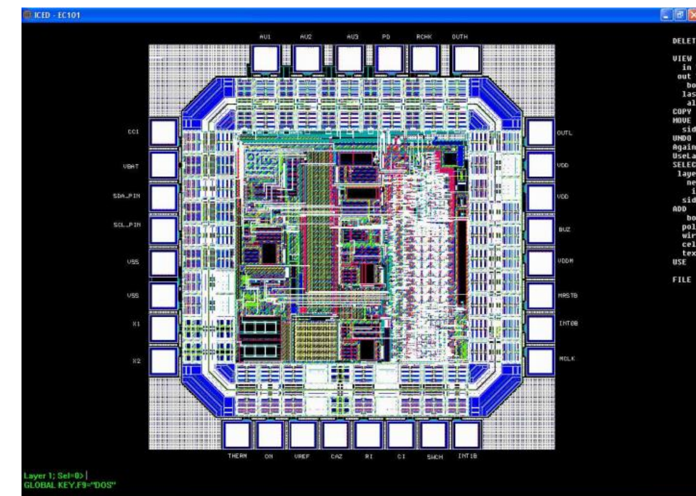
- ❖Big Semiconductor Manufacturers
- ❖Own fabs – very expensive
- ❖Silicon wafers turned into ICs and dies
- ❖Sell wafers to other semiconductor companies
- ❖Main Foundries are TSMC, GlobalFoundries, and UMC.
- ❖Sometimes called pure-play.



Fabless

- ❖Smaller companies – no fab
- ❖Buy wafer from Foundries
- ❖Design and market the chips
- ❖Examples of Fabless: Xilinx, Nvidia, Qualcomm…
- ❖Became more popular after pure-play Foundries





OSATs

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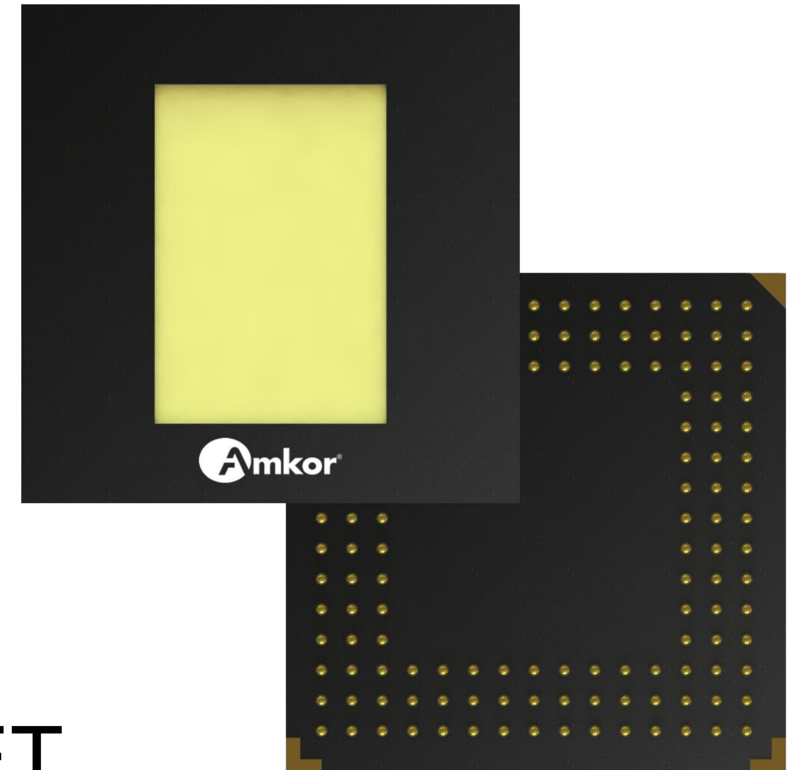
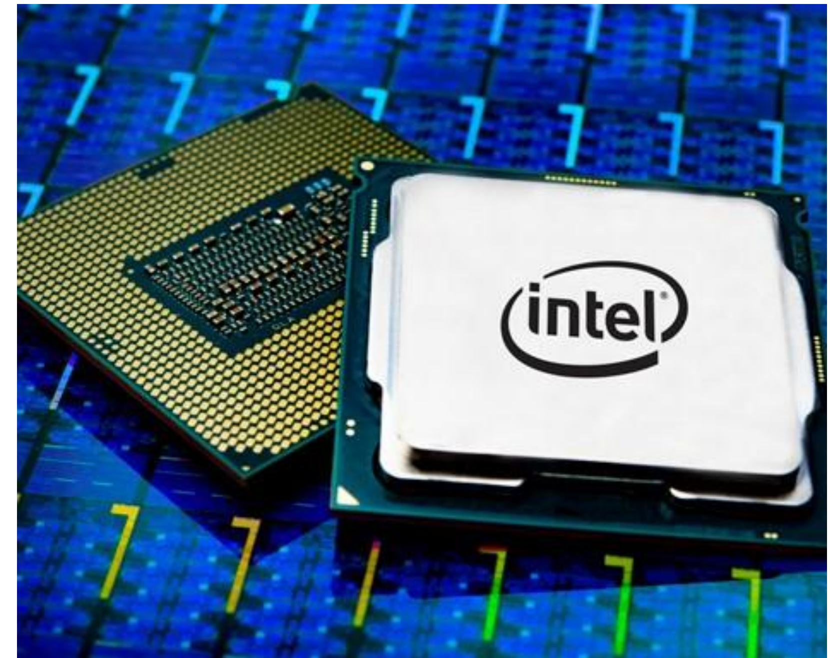
- Outsourced Assembly and Test Companies – Packaging services.
- Work for fabless foundries, or help with overload from other companies
- 37% of worldwide packaging
- Different from one another, different specializations.
- 3D, FBGA, BGA, and other advanced packaging…
- Notable OSATs: ASE Inc, Amkor, JCET…



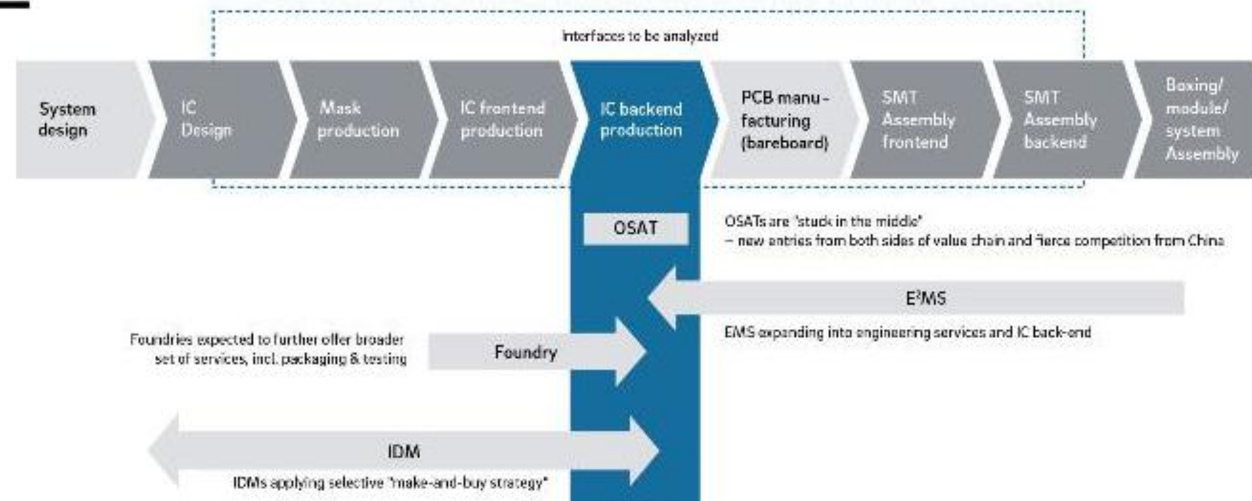
Integrated Device Manufacturers - IDMs

- Full vertical integration
- Design, manufacture, and package
- Traditional approach to market
- Examples of IDMs: Intel, IBM, Texas Instruments



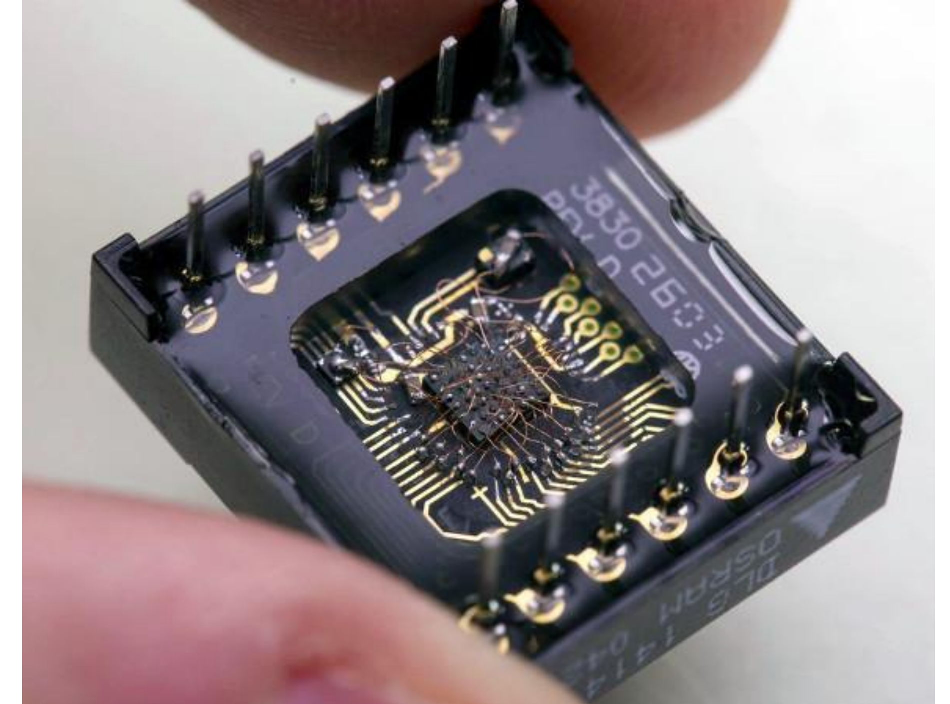
Big Picture

- IDMs do all the work for themselves
- Fabless design chips, Foundries manufacture, and OSATs help package
- Recently, Foundries have started packaging as well – changing domains



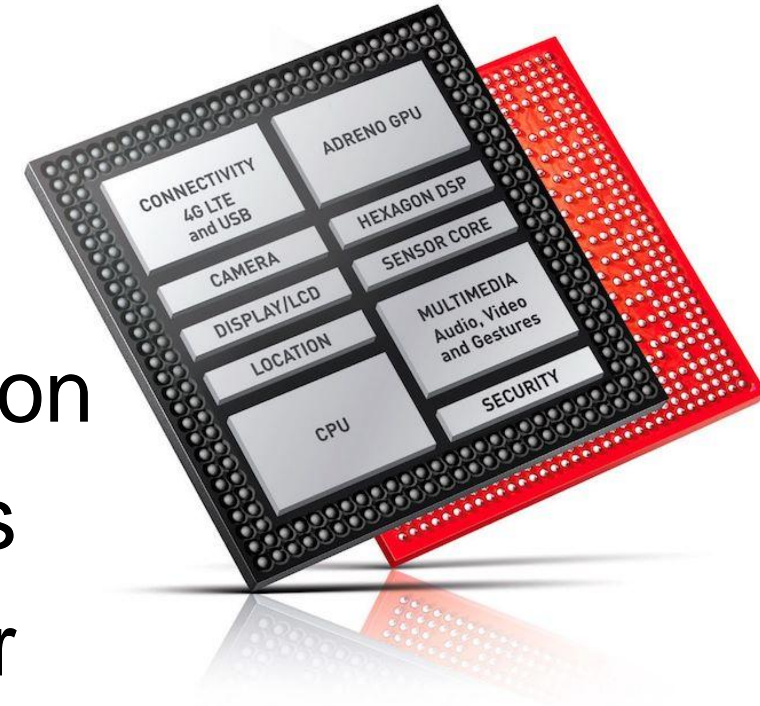
Single Die Packaging

- 1970s - Traditional forms of packaging included a single die into a package
- PGA, BGA, DIP, QFPs…
- When more functionality in a smaller space was needed, SoCs appeared
  - Analog circuits, digital circuits, and optical circuits



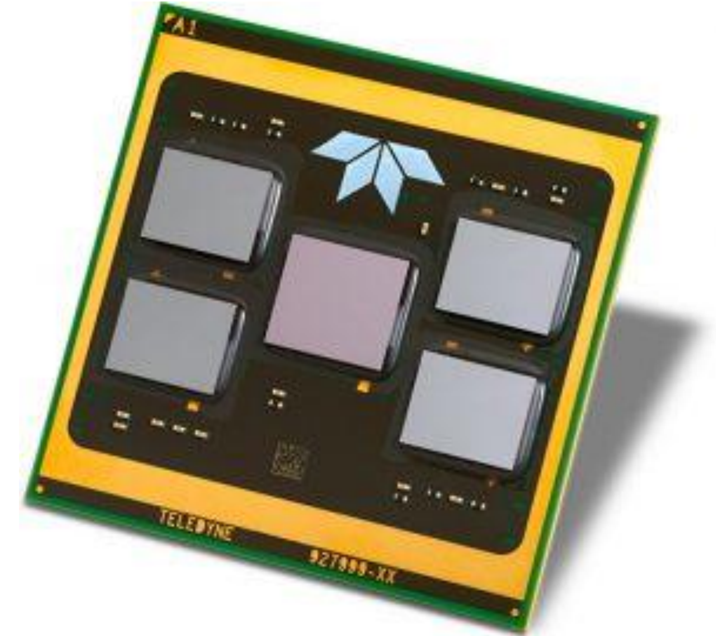
System on Chip - SoC

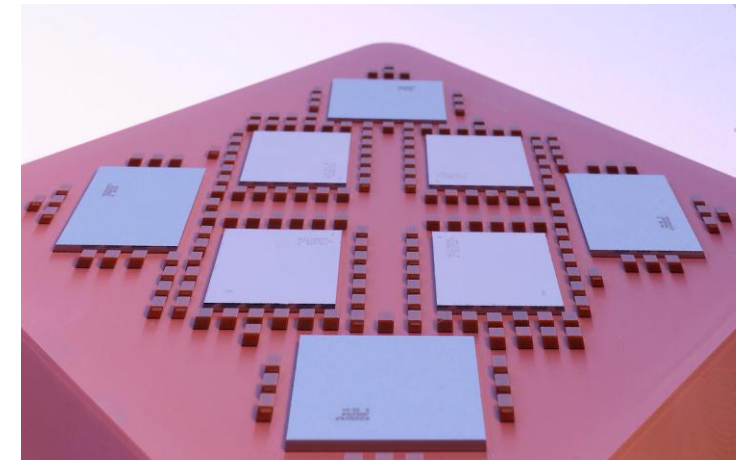
- A whole system on a single chip – most components of a computer
  - Processor, memory, I/Os, DSPs…
- Optimized for power usage, power efficiency, minimized waste heat, and minimized latency – shorter communication
- Made in Foundries – designed by fabless
- No possible upgrading or repairing, lower yield
- Very common in mobile computing – Qualcomm Snapdragon



Multi Chip Module - MCM

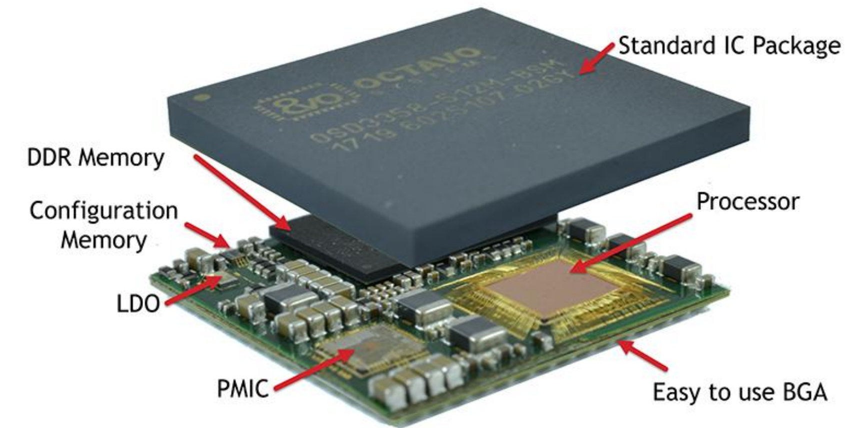
- First developed in the 1980s – another form of multifunctionality
- Gave Foundries and OSATs control over the “design”
- Integrates Homogeneous and Heterogeneous ICs (chiplets) horizontally onto a unifying substrate
- Offered more functionality, simplified design, and higher yield than SoC, but for a higher price

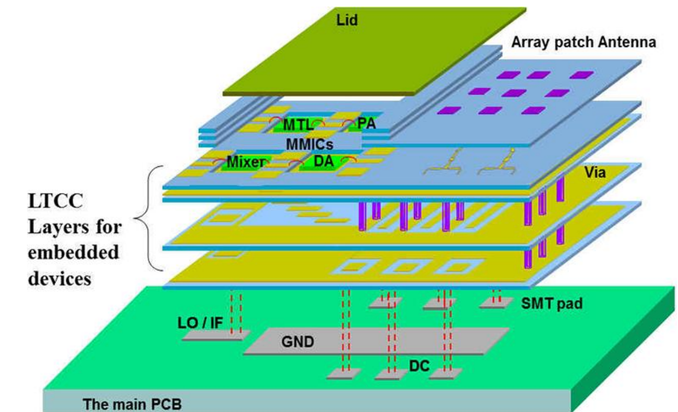




System in Package - SiP

- Stacking of ICs
  - Wire bond => 2.5D and 3D
- Uses interposer layer
- Higher density of transistors
- Advantages:
  - Simple design and verification, low time to market, increased yield, and optimized cost, size, and performance
- Contains active and passive components
- Doesn’t always need a PCB – can house all components needed.





System on Package - SoP

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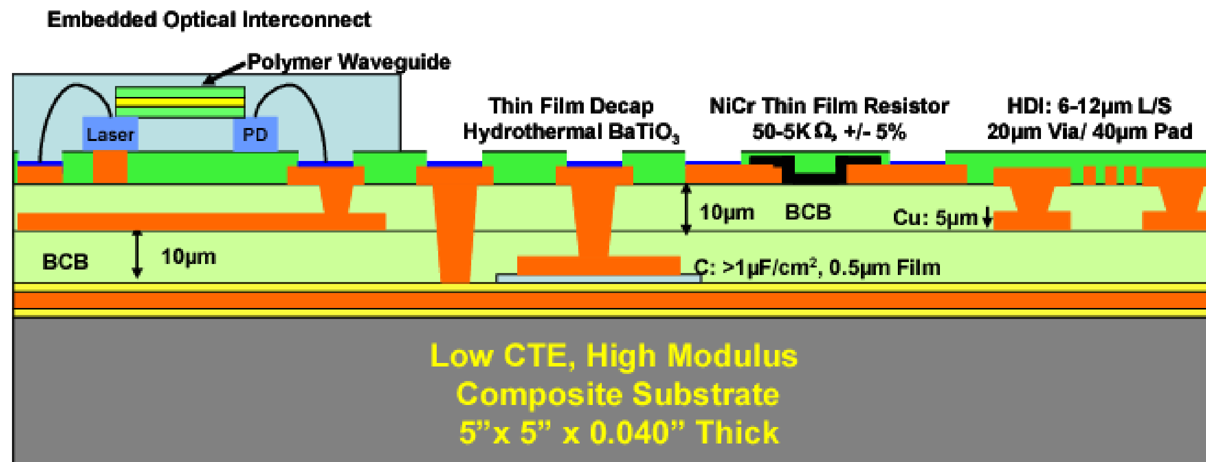
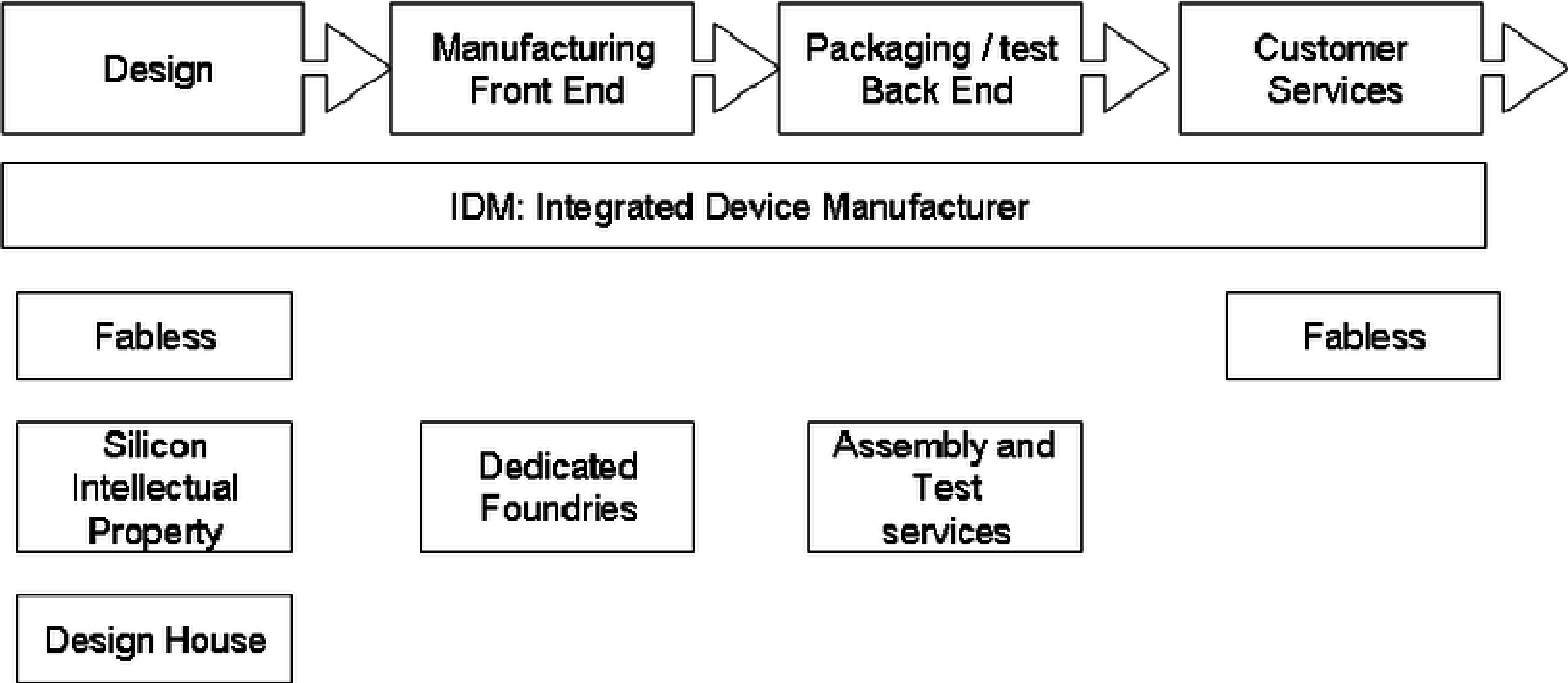
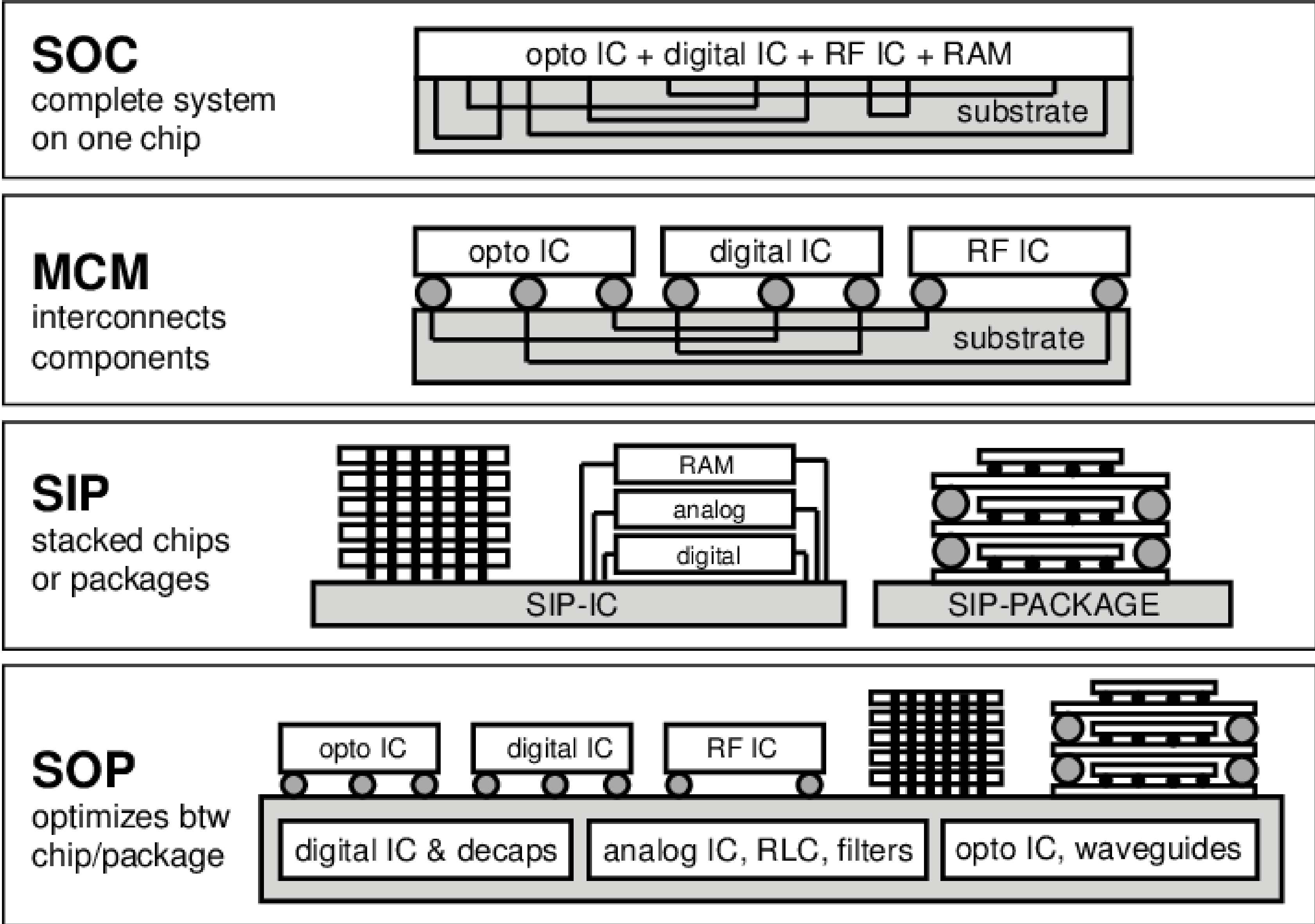
- ❖Evolves from SiP – in development
- ❖Can have components embedded in the substrate, as well as components like SiP or SoC mounted on top.
  - ➢ nanoscale embedded thin-film passive components
- ❖ Follows More than Moore, measures in functions or components/cm^3



Summary



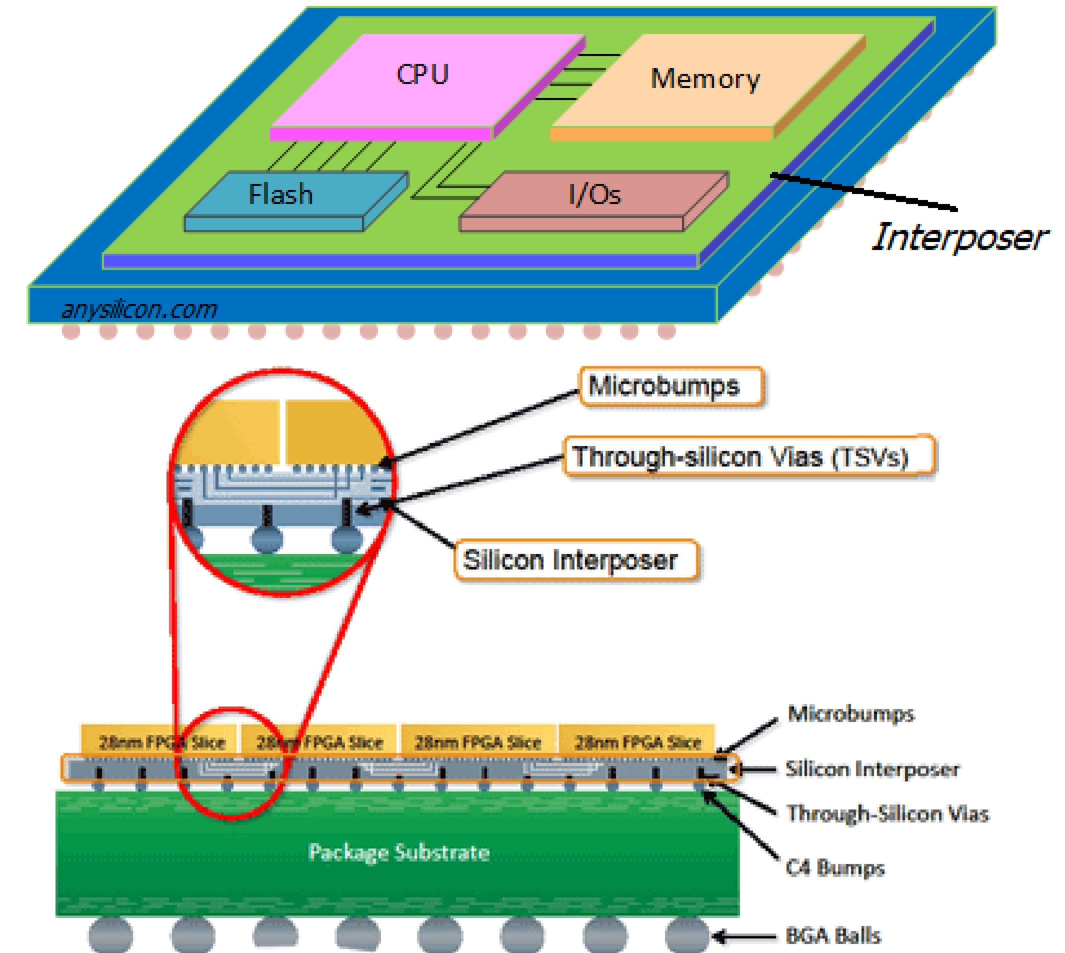
Summary



Silicon Interposer

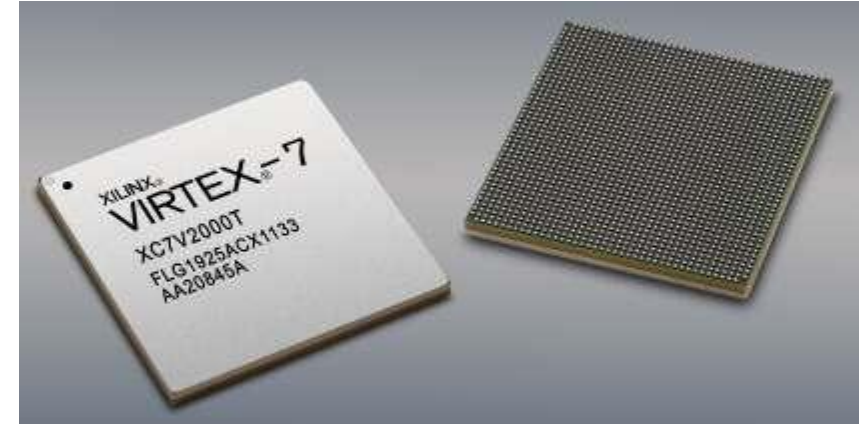
What is a Silicon Interposer

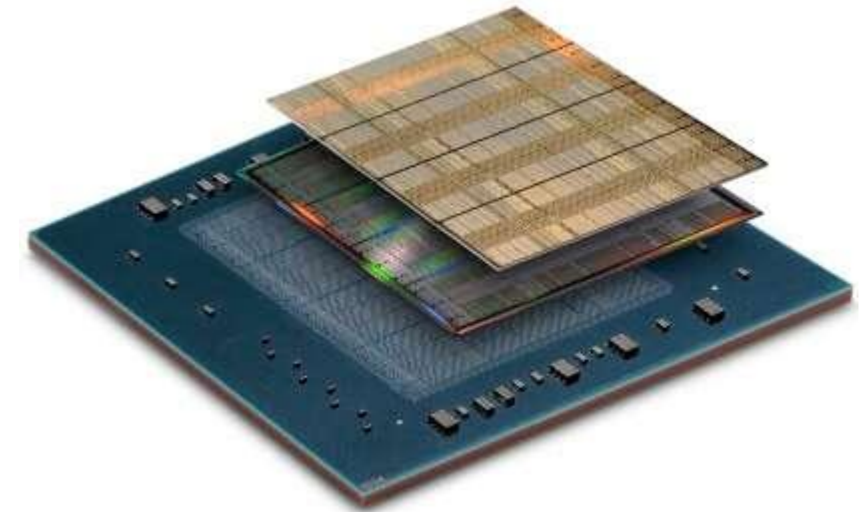
- Silicon layer between substrate and dies
- More than just packaging – also serves as a connection
  - Among dies and to the I/Os
- Uses Through Silicon Vias Technology (TSV)
- Can be Active or Passive
- Fabricated by Foundries



The Need for a Silicon Interposer

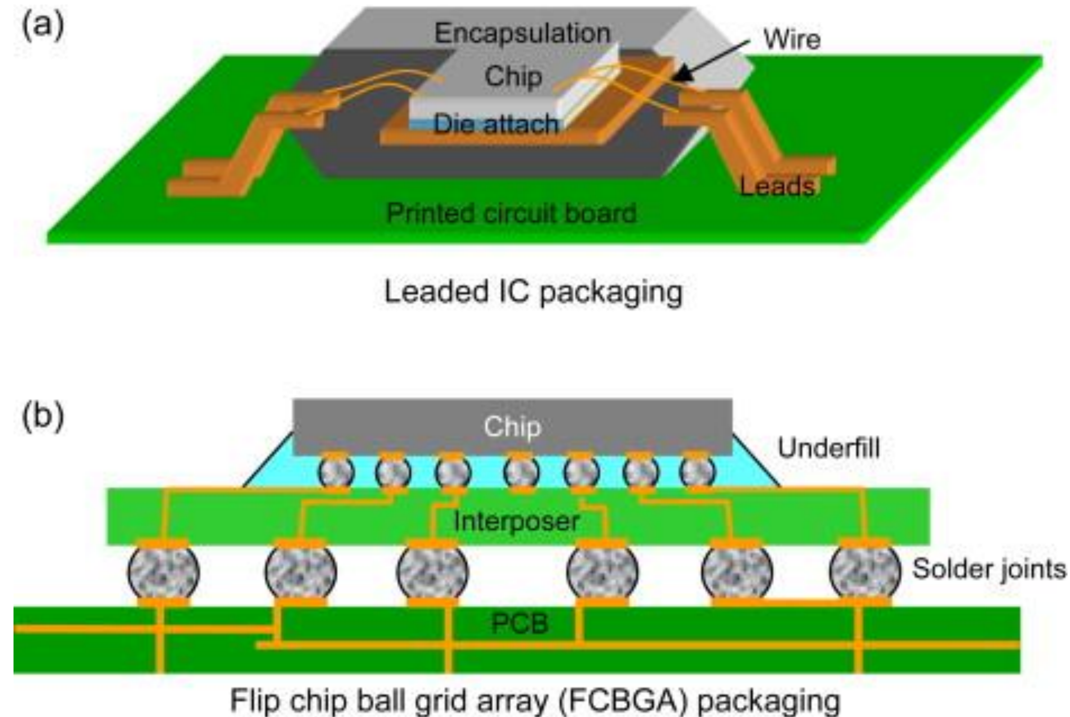
- Need for higher density of interconnections
  - Moore's Law
- Conventional substrates cannot support these chips
- Tested for over 20 years
  - AT&T and IBM worked on it in the 80s
  - Didn't penetrate the market back then
- Today's technology and demands made it possible





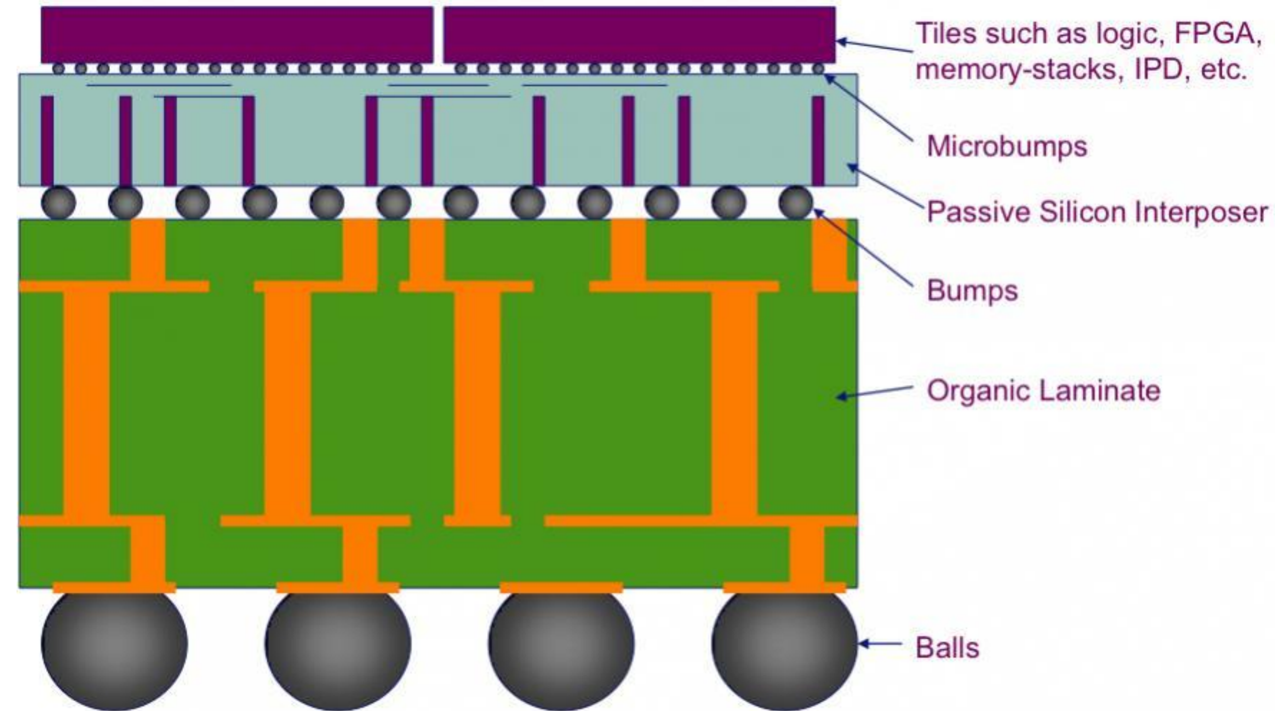
Advantages of the Silicon Interposer

- ❖ High wiring density
- ❖ CTE matched to the silicon die
  - ➢ Interposer to chip specific
- ❖ Excellent electrical and thermal performance, lower power.
  - ➢ Shorter interconnection chip – substrate
- ❖ Lower cost of active devices due to partitioning large die
- ❖ Possibility of integrating passive devices into the substrate



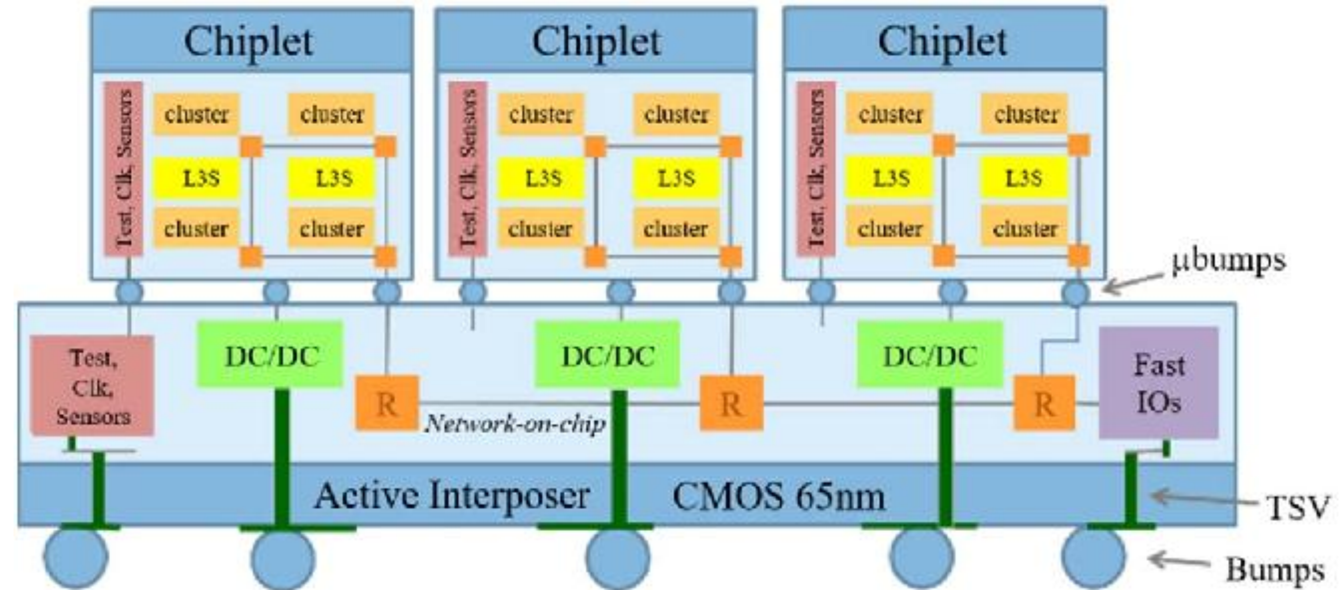
Passive Interposer

- Acts as an interconnection
  - Holds all the dies together
- Communication among the dies in the package and to the I/Os
- No active devices in substrate
- Cannot perform functions
- Higher wiring density



Active Interposer

- ❖ Acts as interconnection
- ❖ Communication among the dies in the package and I/Os
- ❖ Fully functional chips embedded in the silicon substrate
- ❖ Lower TSV density
  - ➢ Keep-Out-Zone

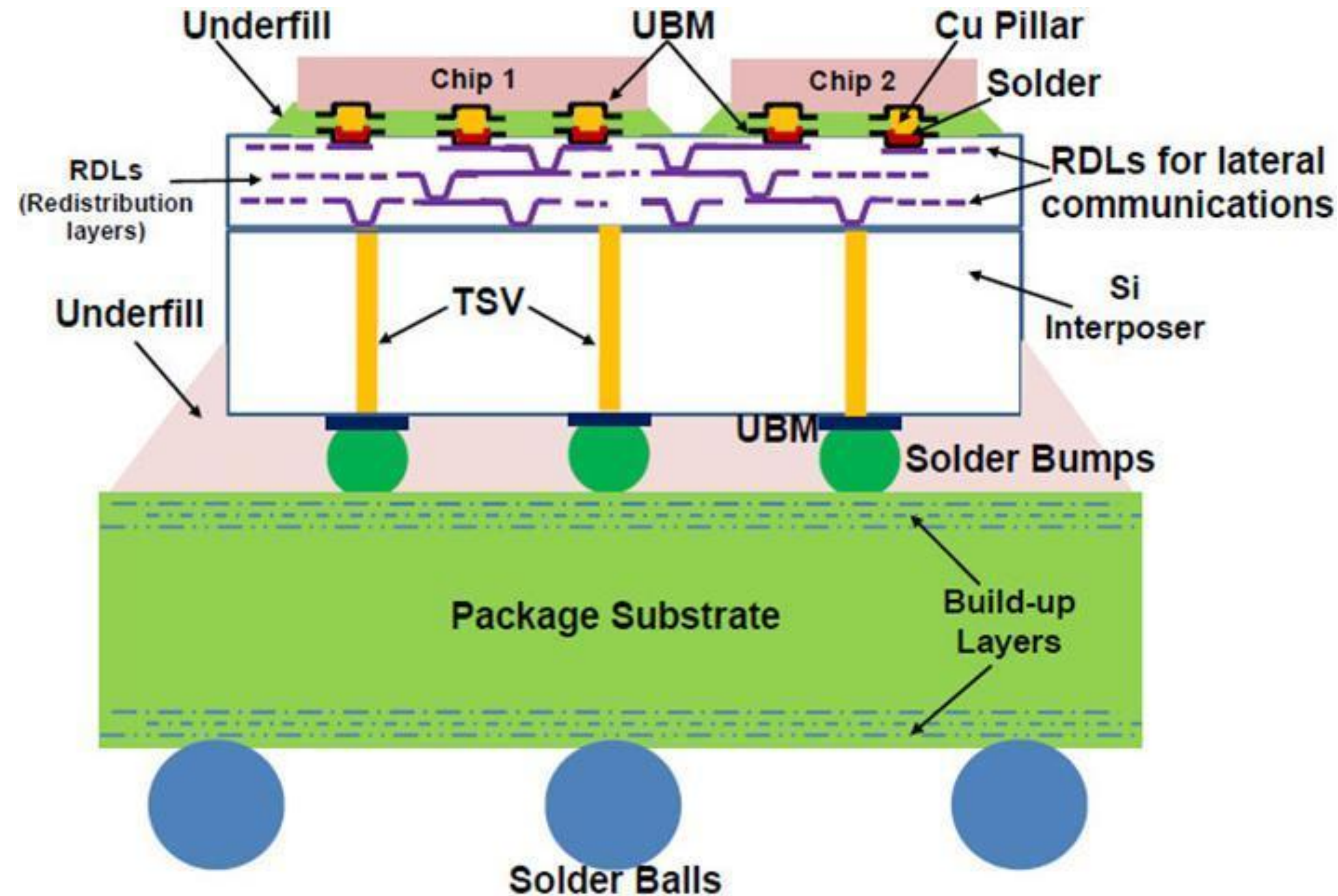


Structure of the Interposer

❖ TSV - Through Silicon Vias

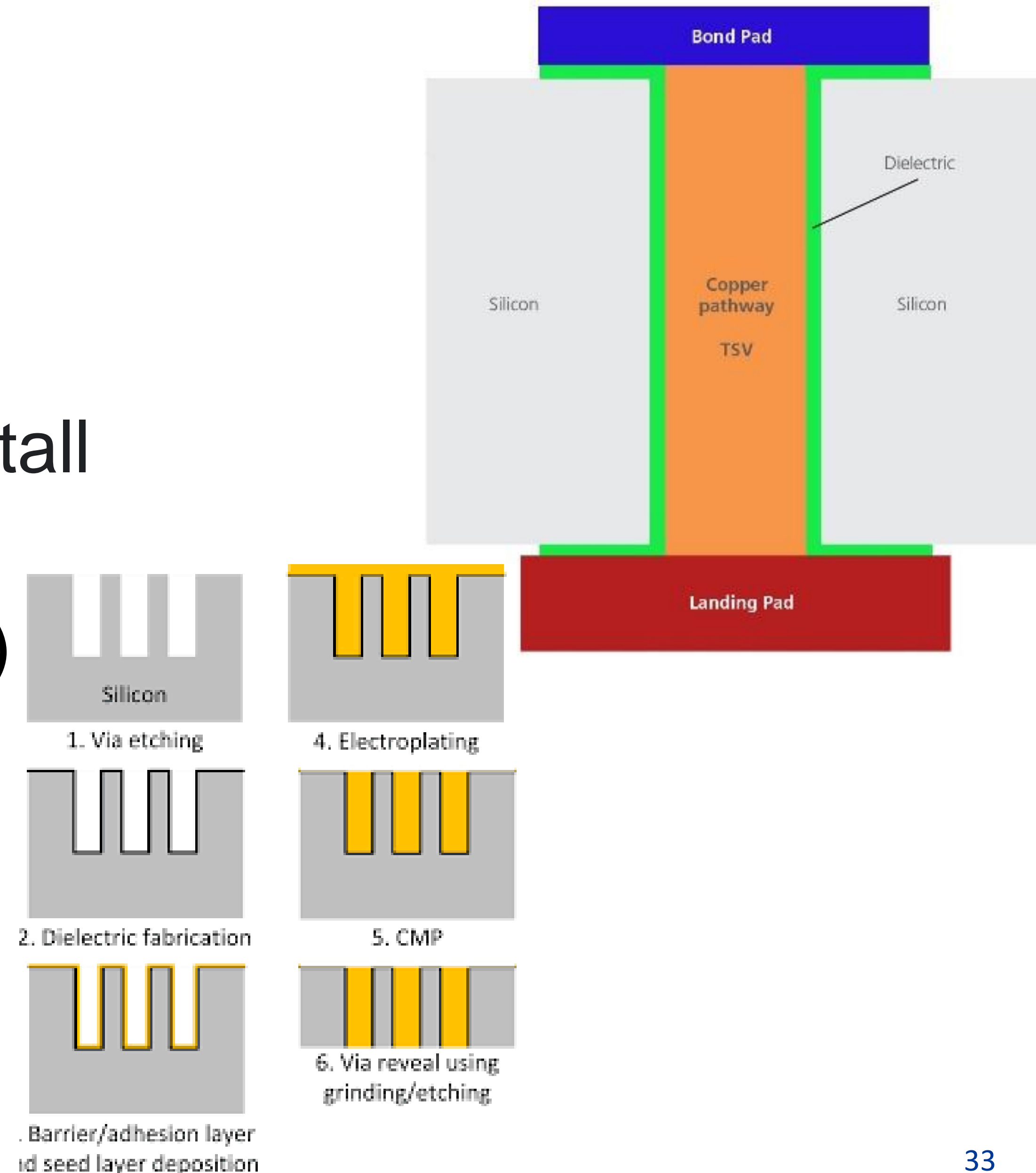
❖ RDL - Redistribution Layer

❖ UBM - Under Bump Metallization



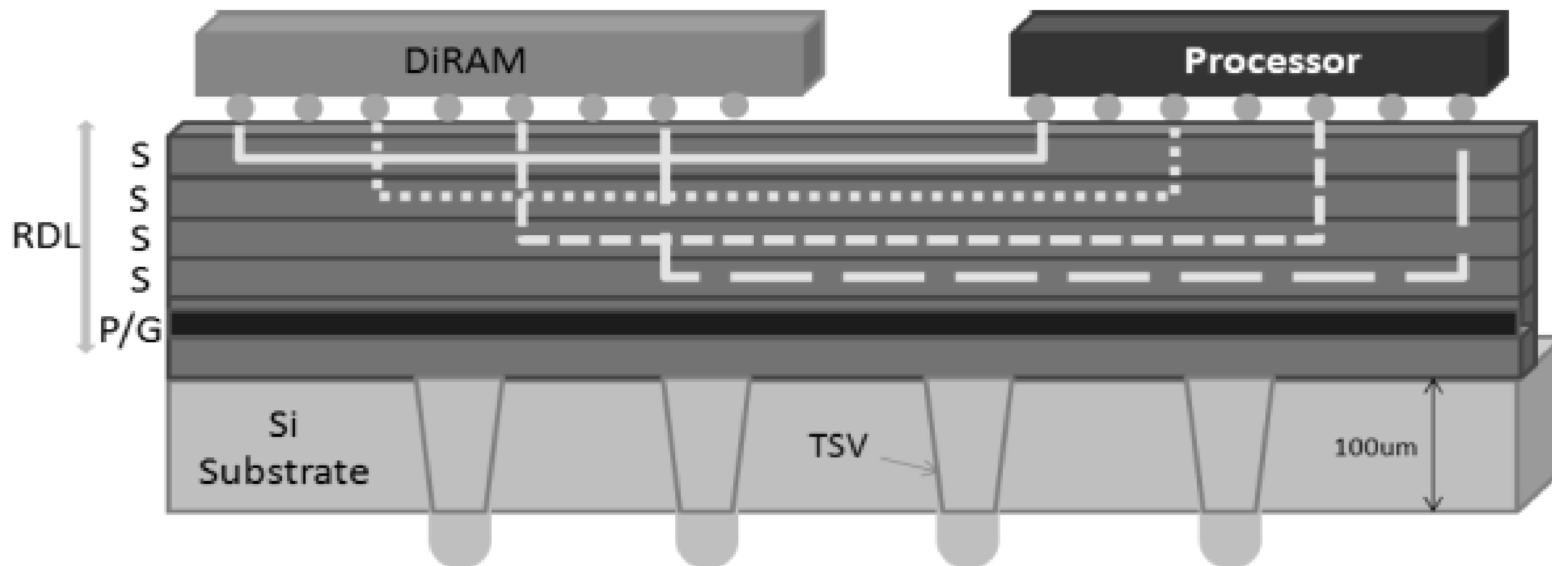
TSV – Through Silicon Vias

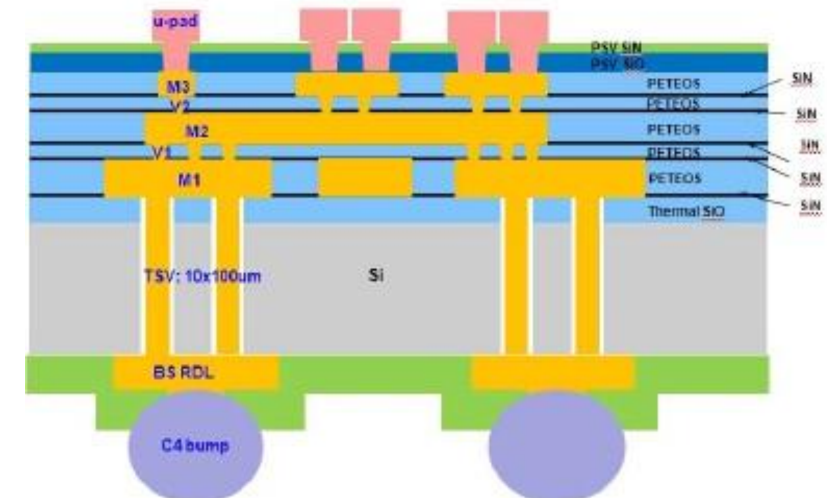
- Vertical pathway through silicon interposer
- Very high aspect ratio
  - Under 20μm wide, up to 200μm tall
- Etching, oxidation, deposition, filling, and CMP (Chemical Metal Polishing)
- Composed of copper pathway, SiO2 isolator, and Barrier
- Keep-Out-Zone in Active Interposer



RDL – Redistribution Layer

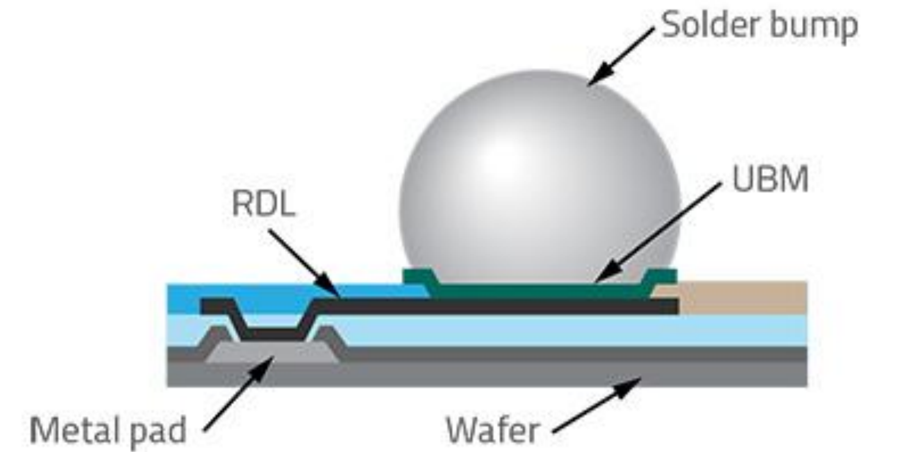
- ❖ Horizontal pathway along the interposer
  - ➢ Connects dies to one another
- ❖ Connects the solder bumps to the TSV by rerouting
- ❖ Copper lines etched into SiO2 layers and polished

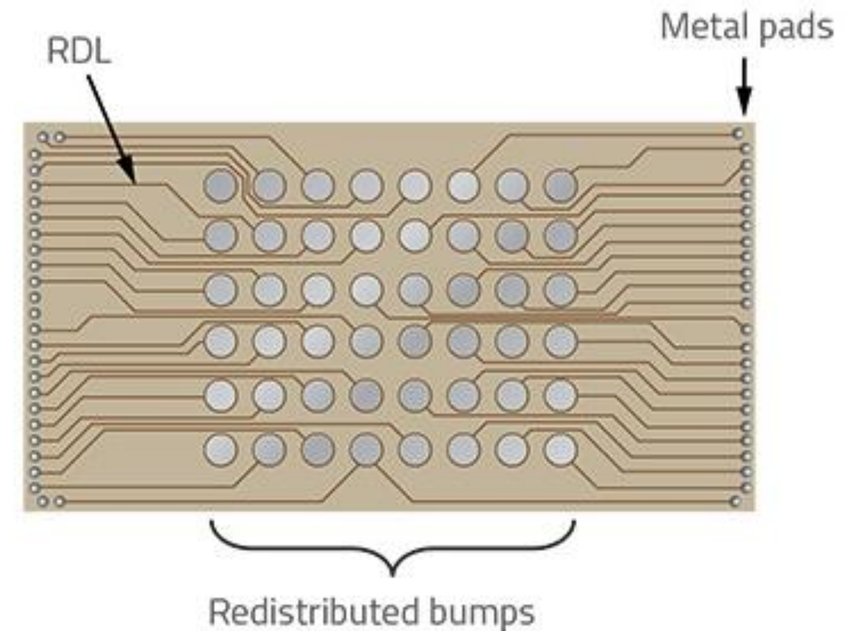




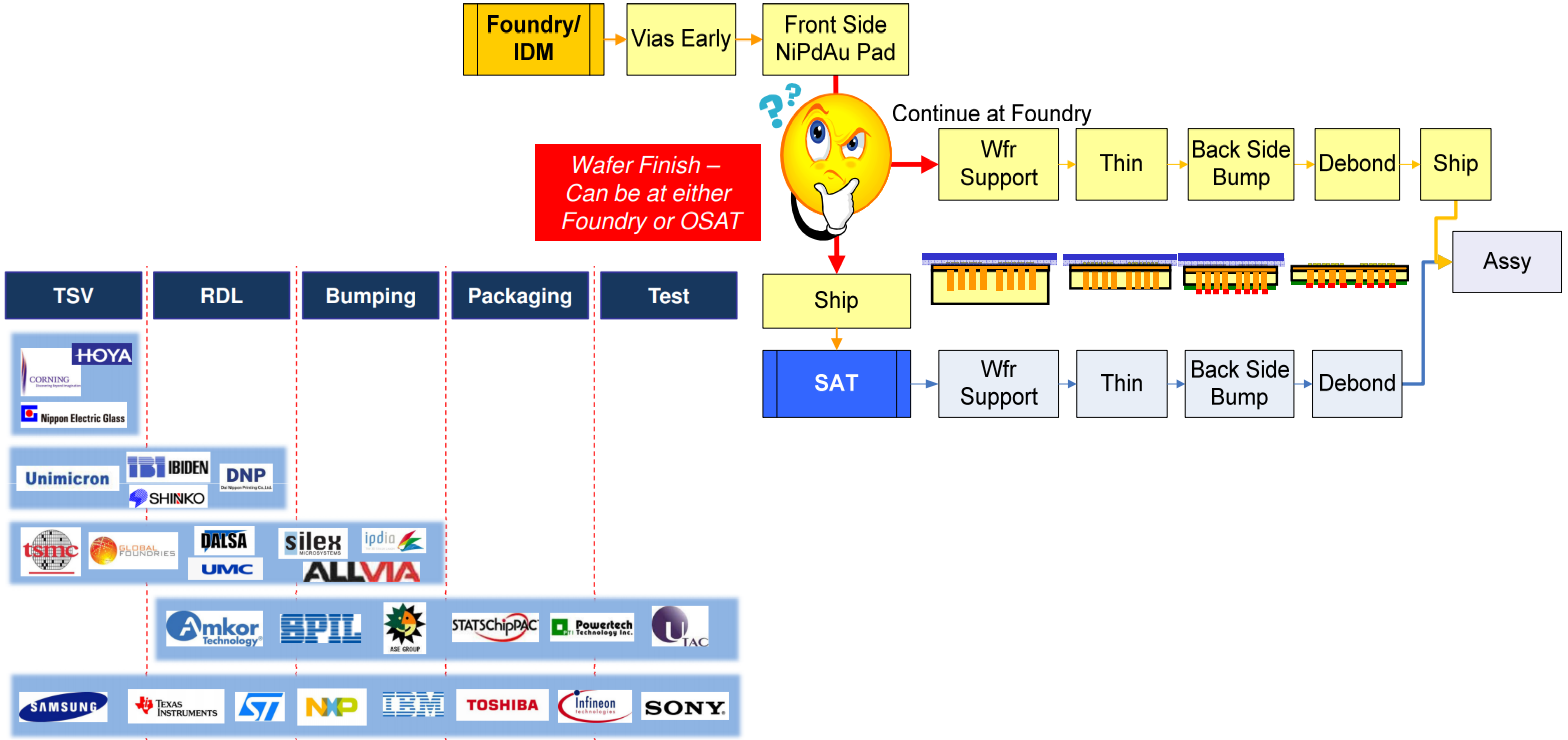
UBM – Under Bump Metallization

- Thin pad connecting the solder bump and the copper in the RDL
- Serves as barrier to stop diffusion
- Acts as a mechanical connection
- Nickel-based UBM widely used





Supply Chain



Summary

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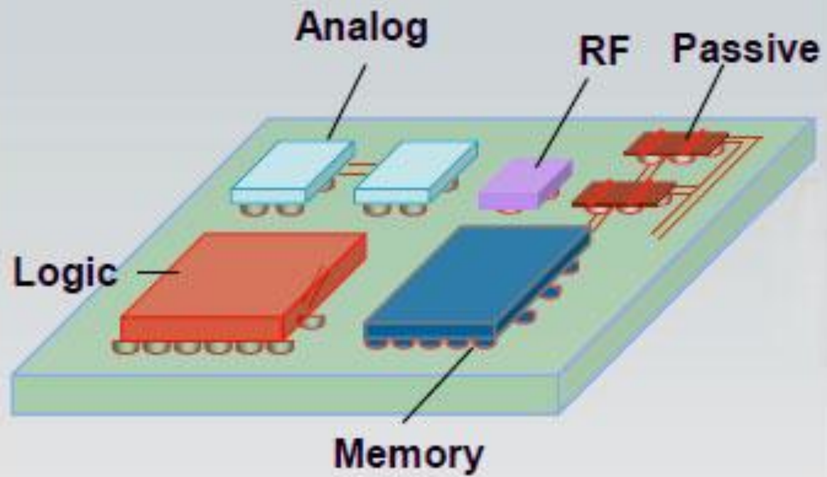
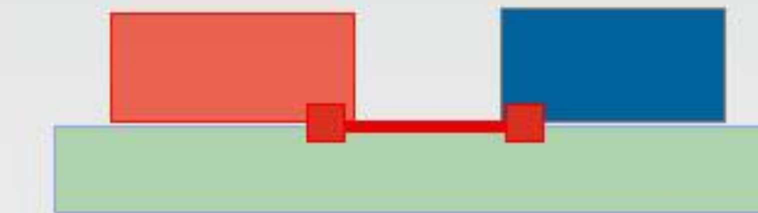
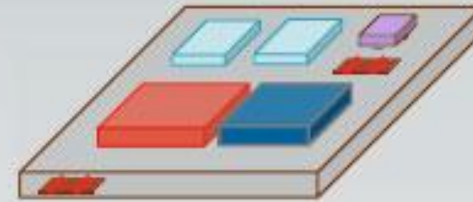
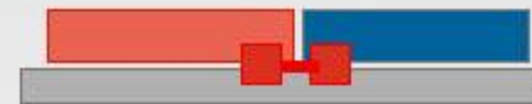
Traditional MCM/PCB → **Silicon Interposer 2.5D**





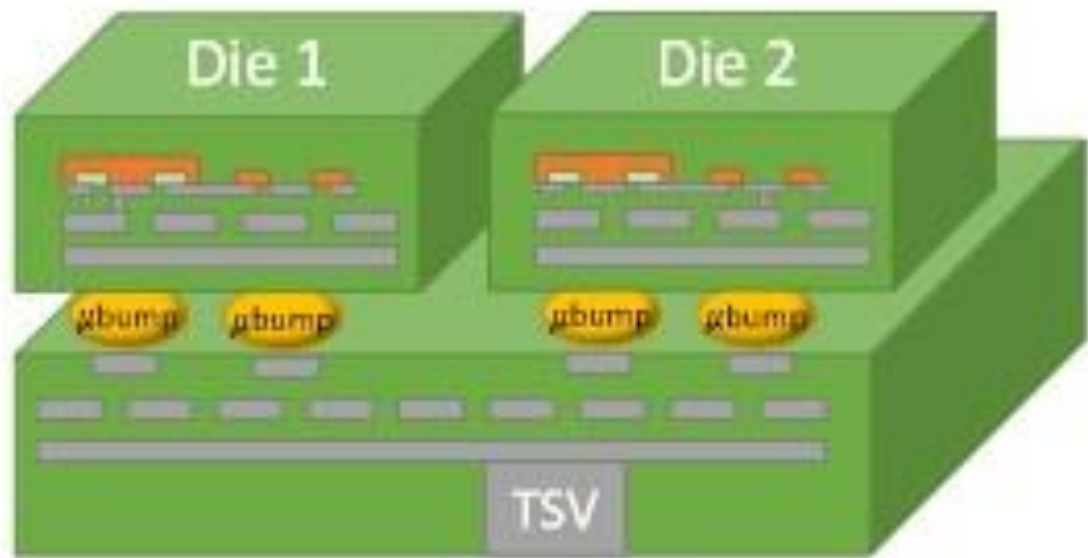
Flipchip + wire bond



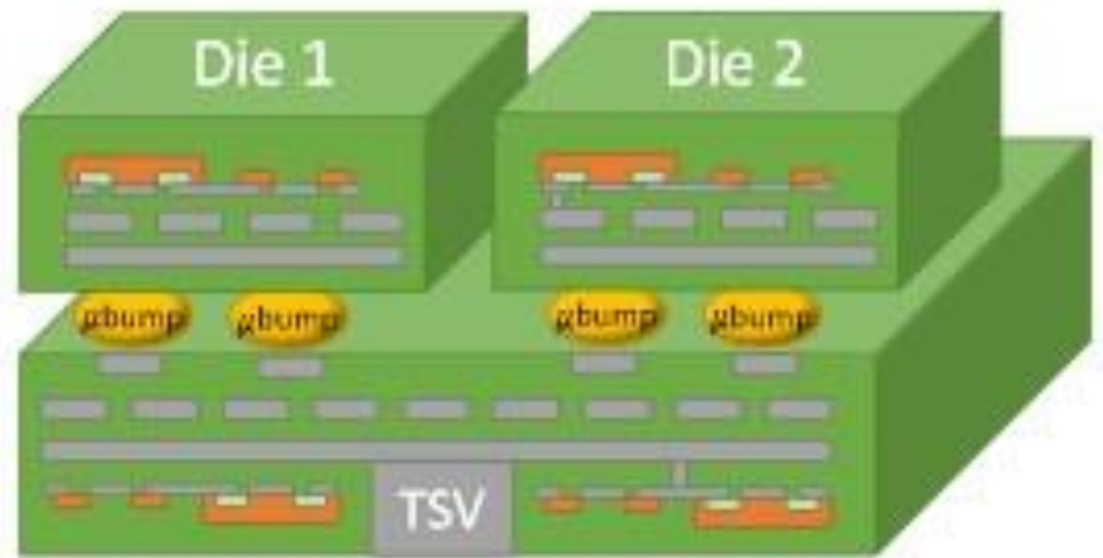


2.5D side-by-side integration with TSVs & silicon interposer

Summary



(a) Passive Interposer



(b) Active Interposer