Sample Preparation and Delayering

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Physical Inspection and Attacks on ElectronicS (PHIKS)
• Physical access to the chip is required
  ➢ Non-Invasive Attack: Observe and manipulating device without any physical harm
  ➢ Invasive Attack: Complete deprocessing of the chip to extract information

Semi-invasive Attack: Removing package keeping the chip structure intact
Probing Attacks

• **Probing**: circumvent encryption by probing at signal wires to extract security sensitive information

*Wet etching*

*Electrical Probing from frontside*

*Nanoprobing*
Backside Probing

- Bulk substrate is mechanically thinned to approximately 25µm
- FIB trench is milled at approximate location of the target signals
- A smaller trench exposes the target traces
- Metal can be deposited to make contacting the circuit with the probing needle easier
Packing and De-packing

Packaging Classification

1. Material
   • Ceramic
     • Expensive
     • Still used in some chips
   • Plastic
2. Packaging
   • Wire bond vs flip chip

De-packing Classification

1. Selective
   • Plasma/reactive ion etching (RIE)
   • Wet chemical etching
2. Non-selective
   • Mechanical cutting and grinding,
     Laser ablation
De-packing

- Acid etching (bare die)
  - Temperature control
  - Sulfuric acid
  - Nitric Acid
  - Mixed acid
  - Rinse acid
- Bond wire protect
  - Maintain integrity of sensitive components

- Mechanical
  - Grinding
  - Polishing

- Laser etching

- Plasma etching
  - Microwaved gas is inciting chemical radicals for isotropic etching
  - The gas mass flow controls the etching rate
  - Can protect silver or copper bond wires
Photonic Inspection/Attack

- Extracting assets through decapsulation and photonic emission
- Frontside and Backside attack
- Tools
  - Depackaging tool
  - Laser/NIR light source required
  - Laser scanning microscope

Semi/invasive Inspection/Attack

- Photonic Side Channel
- Optical Fault Injection
- Optical Probing
The role of optical debug tools in the advancement of semiconductor products & technology is one of the most underappreciated contributors.

- Role in yield enhancement, design debug, & failure analysis

- The implementation of Silicon Immersion Lenses (SIL) pushes to higher NAs to achieve higher resolutions, the depth of focus becomes very narrow.

- A SIL is a fixed focal length lens, the silicon thickness must be tightly controlled.

- Goal: Ultra-thin polishing for visible light (< 700 nm) probing

\[
\frac{\lambda}{2 \sin \theta} \quad 50 - 80 \text{ um} \quad \frac{\lambda}{2n \sin \theta} \quad \frac{\lambda}{2n^2 \sin \theta_1} \quad 2 - 3 \text{ um}
\]
Back Side Thinning

- Ultratech ASAP
- Sample tilt correction is required to improve the planarity during polishing

Before Tilt Alignment

Aligned (with sample tilt controls)
Fine polished

Scratches left which can scatter the photon emissions
The Challenge of Non-Ideal Samples

- The temperature coefficient of expansion difference between the die and the package.
- In general, the shape of the sample is not stationary since the bending strength of the die changes as it gets thinner.
Dynamic Sample Challenges

- Surface profile of one die as it is thinned.
- The sag relaxes ~45 um, from 70 um at full thickness to ~ 25 um when thinned to ~ 10 um.
Approach to Extreme Thinning

Measurement Assembly

50k RPM Spindle
Water Cascade
White LED Lamp
Clean Dry Air
Slurry Ports
Exchange Hardware

Process Assembly

Imaging – NIR and VIS
NIR Spectrometer
VIS Spectrometer

Water Cascade – Recycled
A key element to the silicon removal process is the determination of the remaining silicon thickness. Measurements from highly incoherent surfaces such as the ground silicon surface and the embedded circuit layer.

15 um polished surface

Reference glass

Highly doped: 2E19-1E20

Air

Dielectric

Si

n0
t01
r01
r12
n1
n2

Top surface incoherence

IC interface incoherence
Create a profile map of the silicon substrate to guide the grind process.
Automated Backside Thinning with VarioMill™

- Adaptive 5-axis CNC Tool for Grinding and Polishing of Advanced Package Integrated Circuits
  - Prep for Circuit Edit, Failure Analysis
- In Situ Measurement enables Adaptive Capability
- Tool exchanger provides step-down grinding and multi-tool applications
  - Single Step Polishing
- Adaptive shape and thickness measurement integrated into CNC tool, no external processes

Silicon die 32 x 21 = 672 mm²

Die Relaxes ~ 55 um thinned

Final Sag ~ 125 um @ RST 24 um

Thinned to 24 um RST

Final Polish < 3 nm RMS

Silicon die 32 x 21 = 672 mm²

Initial Sag ~ 180 um @ RST 775 um

Die Relaxes ~ 55 um thinned

Final Sag ~ 125 um @ RST 24 um

22.5 – 26.9 um Final Thickness

Final Polish < 3 nm RMS
Reverse Engineering

Primary Purpose of RE
✓ Analyzing internal structure to extract netlist
✓ Extracting functionality or firmware

Chip Level RE
✓ 5 Steps for complete chip RE

Depacaking
- Selective
- Non-selective

Delayingering
- Plasma/FIB etching
- Wet etching

Imaging
- SEM/Optical

Annotation
- Extract Layer Information

Functionality
- Extract netlist
- VHDL code

Hardware
- Chip
- PCB

Firmware
- FPGA
- Bitstream

Software

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Delayering is an important step to reverse engineering ICs

1. Wet Etching
2. Dry etching

Concerns for successful delayering

- Selectivity
- Etch rate
- Anisotropy (horizontal removal)
- Minimal damage to underlying layers
- Effective removal of reactants and products
Wet Etching

- Acids, bases, oxidizers
- Can be very selective (1000:1)
- Can be very hard to control (rate, direction)
- Take advantage of device structure (etch stops)
- Many premixed off-the-shelf etchants available or can mix your own

<table>
<thead>
<tr>
<th>Material</th>
<th>Chemistry</th>
</tr>
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<tbody>
<tr>
<td>SiO2</td>
<td>HF:NH4OH:H2O</td>
</tr>
<tr>
<td>Al</td>
<td>HCl, H3PO4, NaOH</td>
</tr>
<tr>
<td>Cu</td>
<td>H2O2:H2SO4</td>
</tr>
<tr>
<td>W</td>
<td>H2O2, H2O2:H2SO4</td>
</tr>
<tr>
<td>Au</td>
<td>HCl:HNO3, KI</td>
</tr>
<tr>
<td>Ti</td>
<td>H2O2:H2SO4, HF:HNO3</td>
</tr>
</tbody>
</table>

many more and many variations...
Advanced Etching

- Laser
- Ion beam milling

![Advanced Etching Diagram](image-url)
1. Dry Plasma etch to remove passivation and see the metal layers
2. Wet etch to remove aluminum
3. Polishing to remove the barrier
4. Dry plasma etch to expose the next metal layer
5. Wet etch that removes Al but does not attack the tungsten via
Delaying – Case study

DRY ETCH PASSIVATION (NITRIDE, OXIDE) - RIE:CF4/CHF3/O2

WET ETCH M4 - NaOH

POLISH M4 BARRIER - Silica Slurry

DRY ETCH IMD3 - RIE:CF4/CHF3/O2
Challenges

- Delamination
- Thin layers, half layers
- Planarity
- Material removal rates
  - Metal removal (grain boundaries)
- Pattern density
- Die size (thickness, length, width)
- Not enough parts
PFIB Delayering
Readings and Videos

- [https://www.youtube.com/watch?v=tnY7UVyaFiQ&list=PLe7niMUMEviOyD05aEA08lWVau_sDEScH&index=11&t=0s](https://www.youtube.com/watch?v=tnY7UVyaFiQ&list=PLe7niMUMEviOyD05aEA08lWVau_sDEScH&index=11&t=0s)
- [https://www.youtube.com/watch?v=oQzF-di-JQo](https://www.youtube.com/watch?v=oQzF-di-JQo)