

# Sample Preparation and Delayering

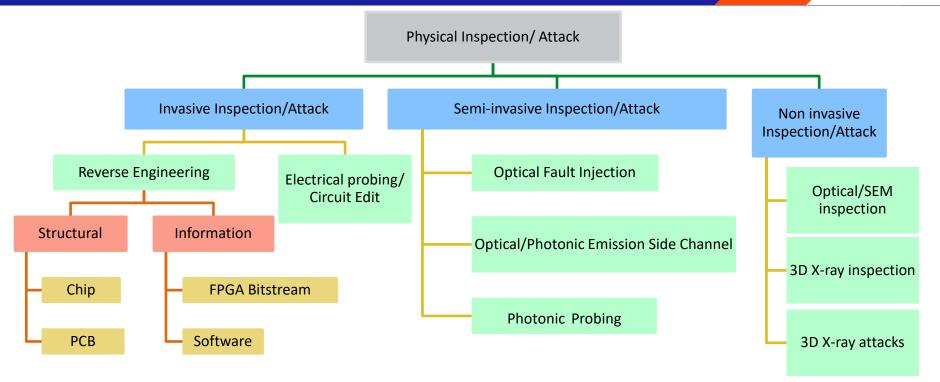
# Navid Asadi

### **Physical Inspection and AttacKs on ElectronicS (PHIKS)**



## **Physical Inspection/Attack**





- Physical access to the chip is required
  - > Non-Invasive Attack: Observe and manipulating device without any physical harm
  - Invasive Attack: Complete deprocessing of the chip to extract information

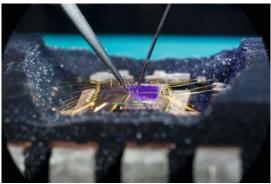


Semi-invasive Attack: Removing package keeping the chip structure intact All Rights Reserved

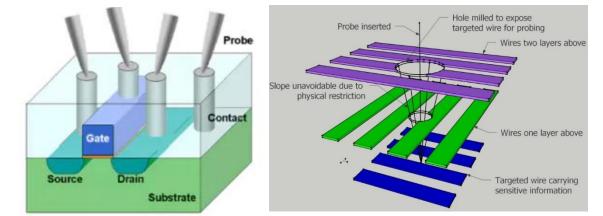
## **Probing Attacks**



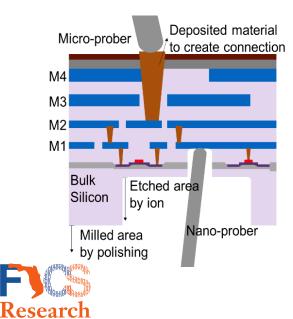
• Probing: circumvent encryption by probing at signal wires to extract security sensitive information

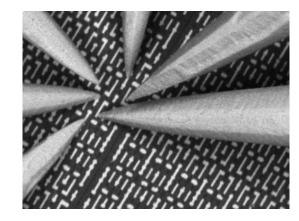


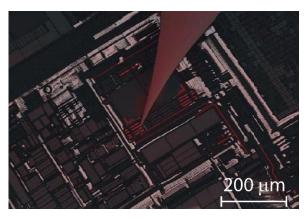
Wet etching



### Electrical Probing from frontside



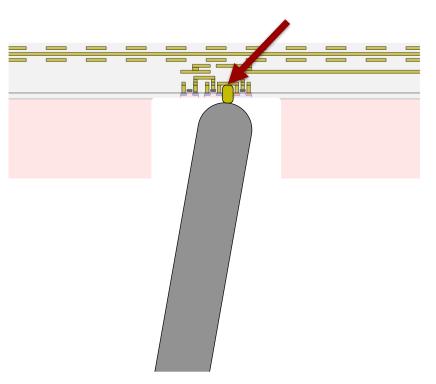




Nanoprobing

# **Backside Probing**





- Bulk substrate is mechanically thinned to approximately 25µm
- FIB trench is milled at approximate location of the target signals
- A smaller trench exposes the target traces
- Metal can be deposited to make contacting the circuit with the probing needle easier



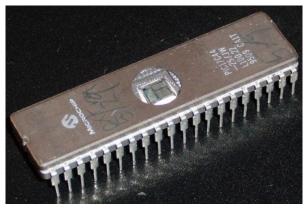
# **Packing and De-packing**

### **Packaging Classification**

- 1. Material
  - Ceramic
    - Expensive
    - Still used in some chips
  - Plastic
- 2. Packaging
  - Wire bond vs flip chip



Plastic

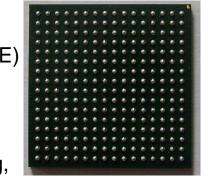


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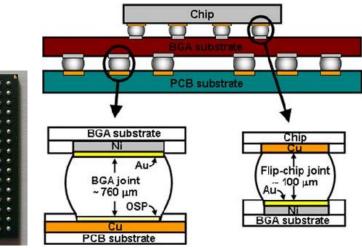
Ceramic

### **De-packing Classification**

- 1. Selective
  - Plasma/reactive ion etching (RIE)
  - Wet chemical etching
- 2. Non-selective
  - Mechanical cutting and grinding, Laser ablation



**BGA** 

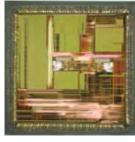


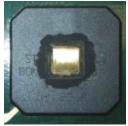


# **De-packing**

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- Acid etching (bare die)
  - Temperature control
  - Sulfuric acid ٠
  - Nitric Acid ٠
  - Mixed acid
  - **Rinse** acid
- Bond wire protect
  - Maintain integrity of ٠ sensitive components





- Mechanical
  - Grinding
  - Polishing



Laser etching



- Plasma etching
  - Microwaved gas is inciting chemical radicals for isotropic etching
  - The gas mass flow controls the etching rate
  - Can protect silver or copper bod wires







## **Photonic Inspection/Attack**



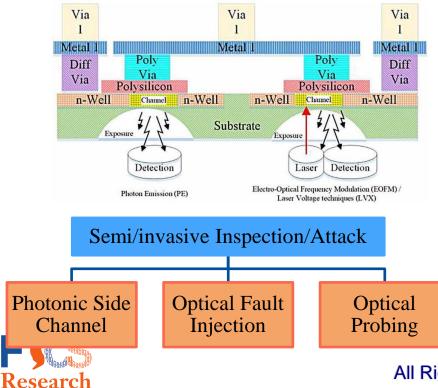
CCD

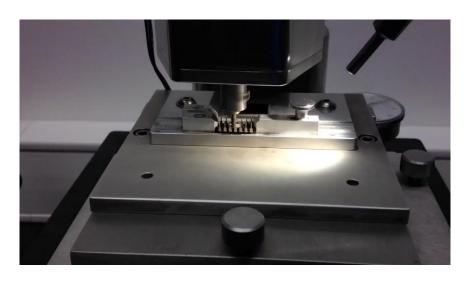
**Black Body** 

or Photon

Emission

- Extracting assets through decapsulation and photonic emission
- Frontside and Backside attack
- Tools
  - Depackaging tool
  - Laser/NIR light source required
  - Laser scanning microscope





ase

- Photon Emission
- Rise and Fall Events of Digital Signal Pattern
  - Modulation
- Modulation of reflected light by device operation: Contactless Probing
- Laser Stimulated Current or Voltage Sources: Delay / Fault Injection

#### Laser Stimulated Electrical Signal

Nanoscale Debug & Diagnosis I TU Berlin

Bulk

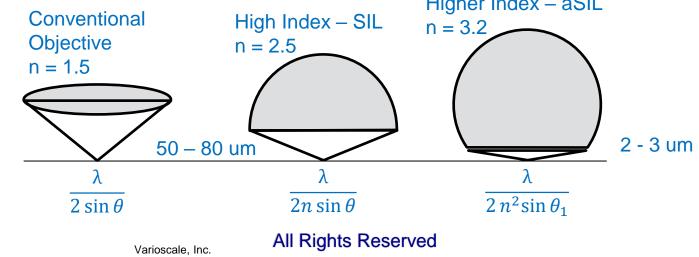
Si

## The Drive for Ultra Thin

Research

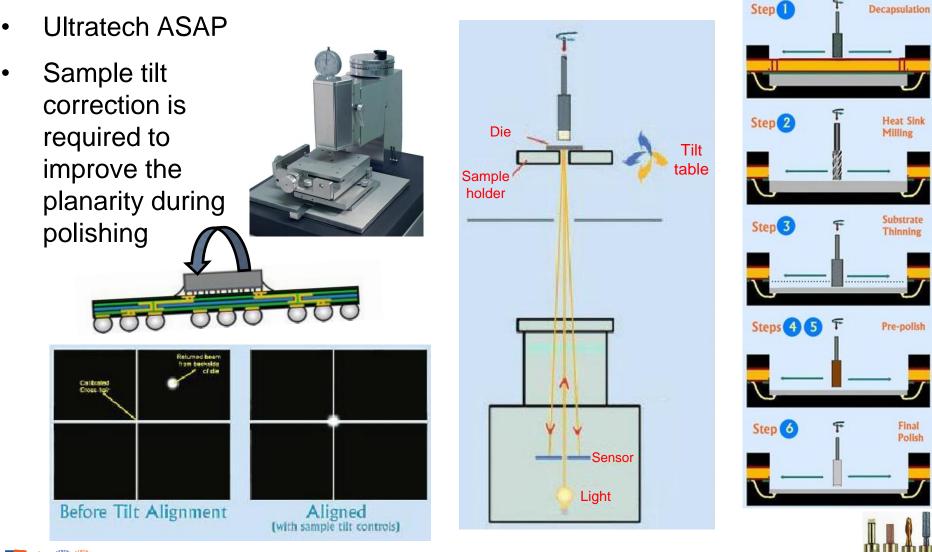


- The role of optical debug tools in the advancement of semiconductor products & technology is one of the most underappreciated contributors.
  - Role in yield enhancement, design debug, & failure analysis
- The implementation of Silicon Immersion Lenses SIL push to higher NAs, to achieve higher resolutions, the depth of focus becomes very narrow.
  - A SIL is a fixed focal length lens, the silicon thickness must be tightly controlled.
- Goal: Ultra-thin polishing for visible light (< 700 nm) probing Higher Index – aSIL



## **Back Side Thinning**





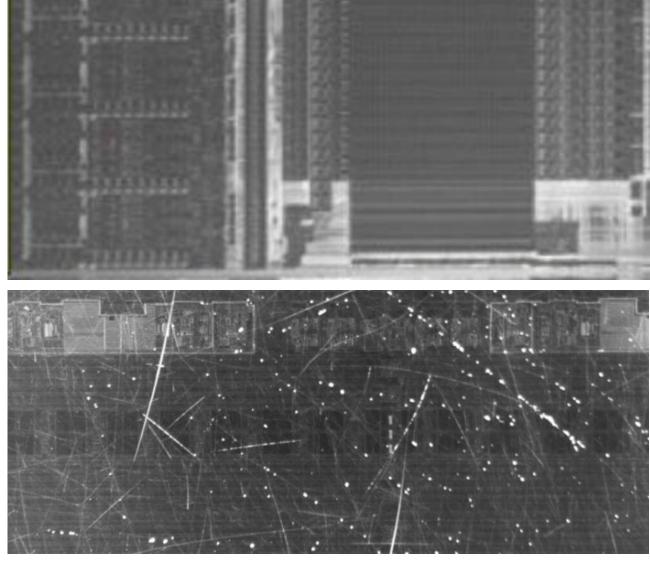


## **PEM Image Examples**



Fine polished

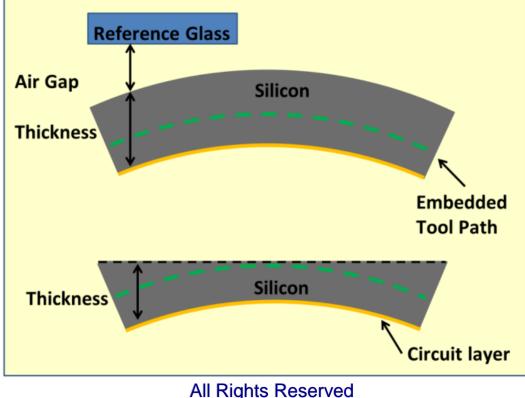
Scratches left which can scatter the photon emissions







- The temperature coefficient of expansion difference between the die and the package.
- In general, the shape of the sample is not stationary since the bending strength of the die changes as it gets thinner

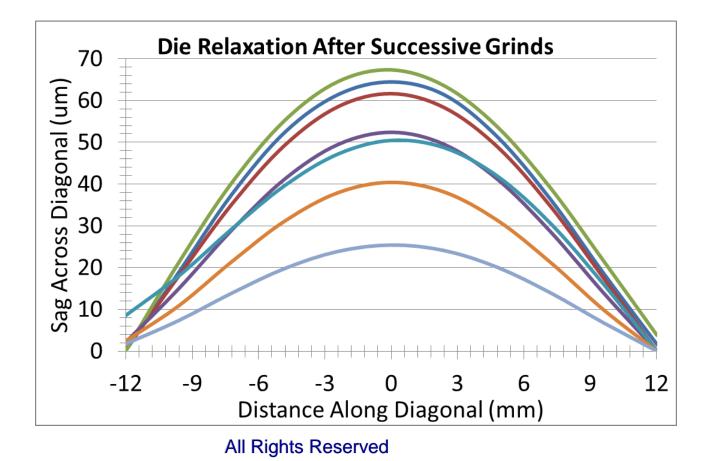




## **Dynamic Sample Challenges**



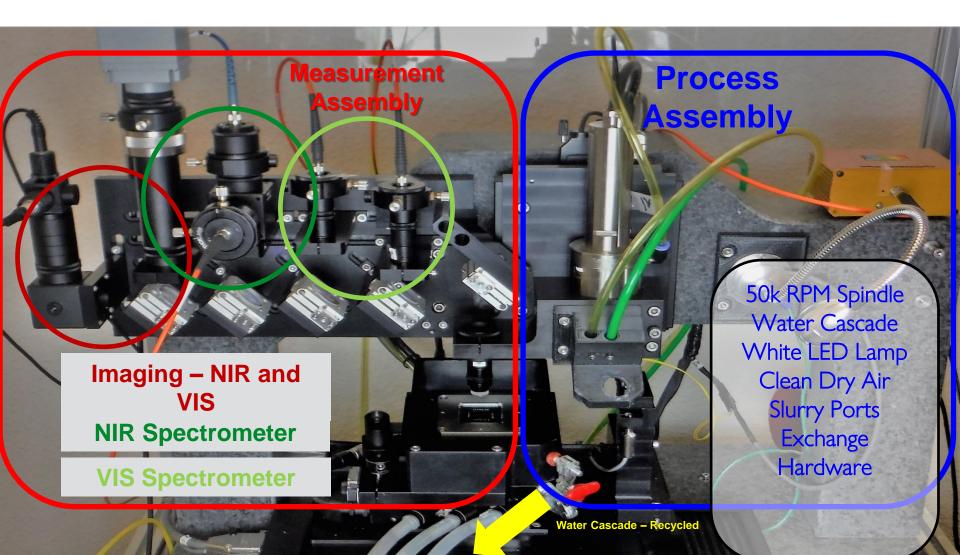
- Surface profile of one die as it is thinned.
- The sag relaxes ~45 um, from 70 um at full thickness to ~ 25 um when thinned to ~ 10 um.





## **Approach to Extreme Thinning**



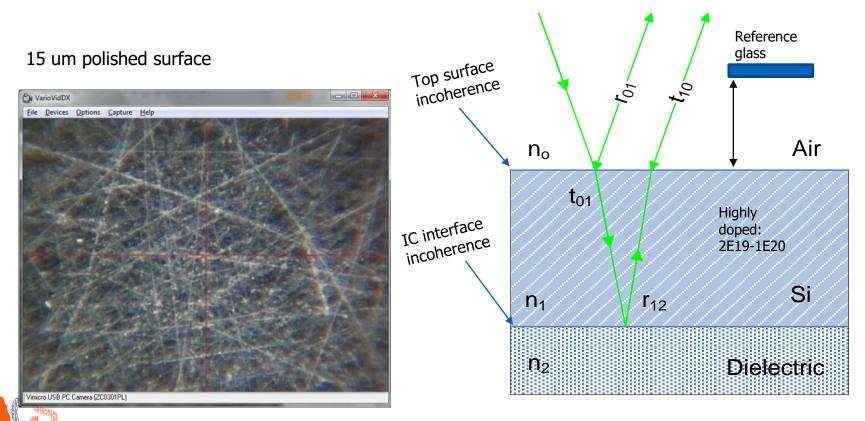


Research

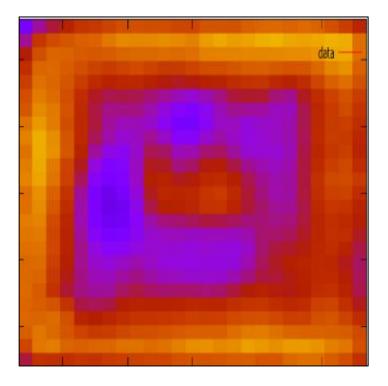
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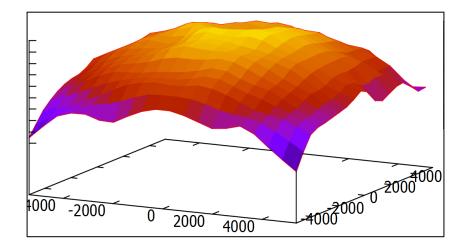
A key element to the silicon removal process is the determination of the remaining silicon thickness.

Measurements from highly incoherent surfaces such as the ground silicon surface and the embedded circuit layer.



Create a profile map of the silicon substrate to guide the grind process.





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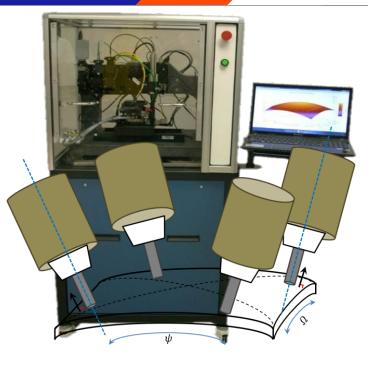
### Automated Backside Thinning with VarioMill™

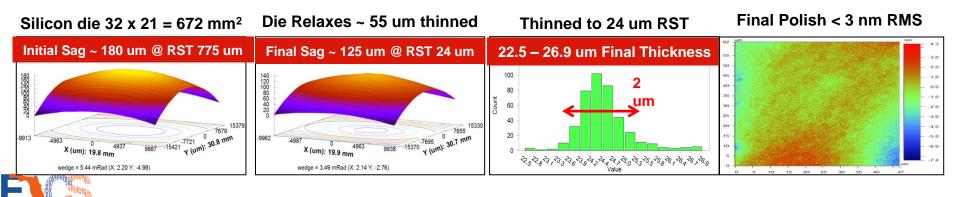


- Adaptive 5-axis CNC Tool for Grinding and Polishing of Advanced Package Integrated Circuits
  - Prep for Circuit Edit, Failure Analysis
- In Situ Measurement enables Adaptive Capability
- Tool exchanger provides step-down grinding and multi-tool applications
  - Single Step Polishing

Kesear

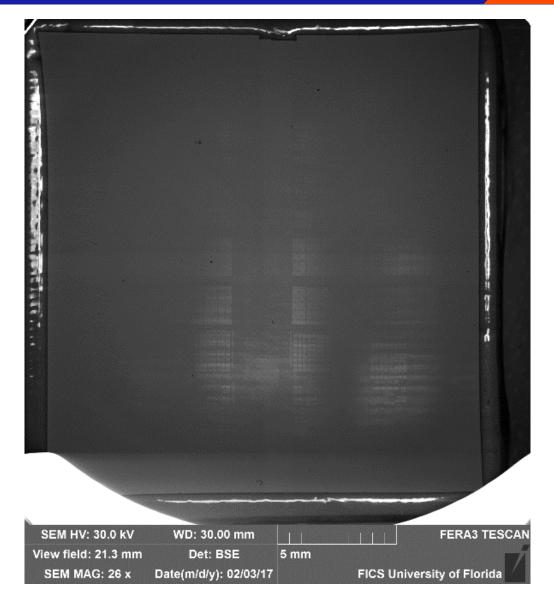
 Adaptive shape and thickness measurement integrated into CNC tool, no external processes





# **Back side Ultra thinned**

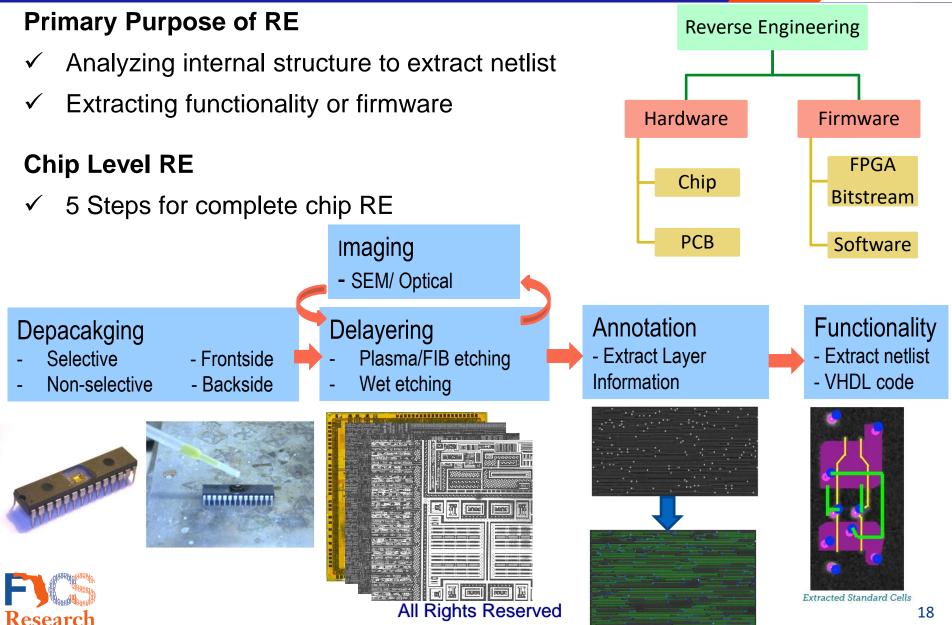






## **Reverse Engineering**





# Delayering

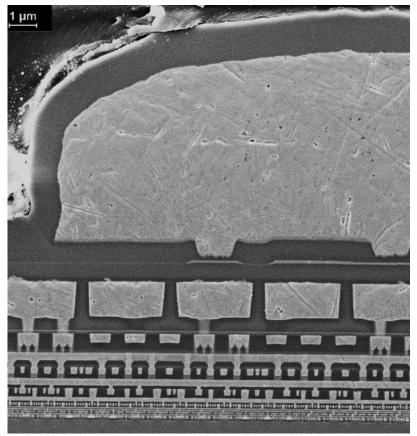


Delayering is an important step to reverse engineering ICs

- 1. Wet Etching
- 2. Dry etching

Concerns for successful delayering

- Selectivity
- Etch rate
- Anisotropy (horizontal removal)
- Minimal damage to underlying layers
- Effective removal of reactants and products



Cross section of a 14 nm Intel skylake i7 cp.



# Wet Etching



- Acids, bases, oxidizers
- Can be very selective (1000:1)
- Can be very hard to control (rate, direction)
- Take advantage of device structure (etch stops)
- Many premixed off-the-shelf etchants available or can mix your own

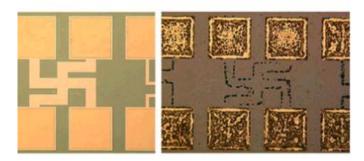
Mat	erial	Chemistry
SiO	2	HF:NH4OH:H20
AI		HCI, H3PO4, NaOH
Cu		H2O2:H2SO4
w		H2O2, H2O2:H2SO4
Au		HCI:HNO3, KI
Ti		H2O2:H2SO4, HF:HNO3
a and a second s		many more and many variations
esearch		All Rights Reserved

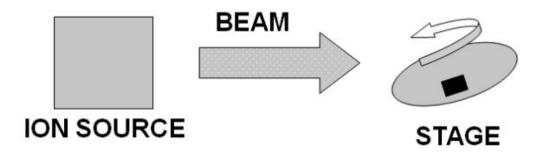
# **Advanced Etching**

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- Laser
- Ion beam milling





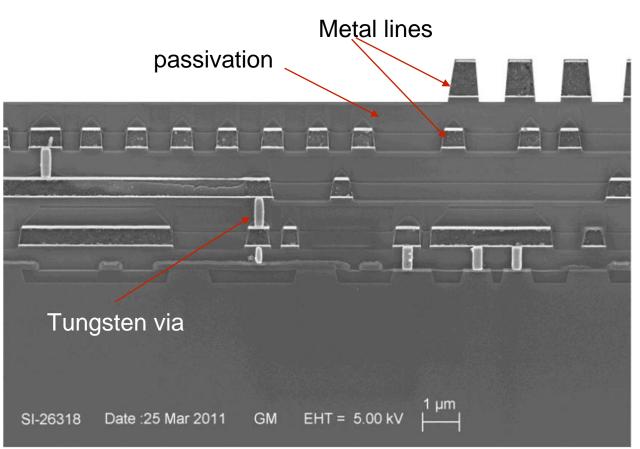




# **Delayering – Case study**



- Dry Plasma etch to remove passivation and see the metal layers
- 2. Wet etch to remove aluminum
- 3. Polishing to remove the barrier
- Dry plasma etch to expose the next metal layer
- Wet etch that removes AI but does not attack the tungsten via

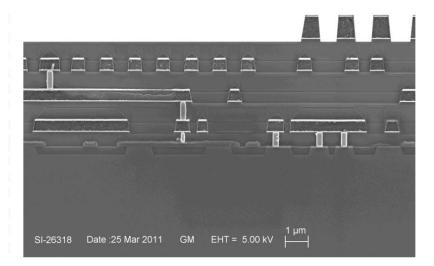


DRY ETCH PASSIVATION (NITRIDE, OXIDE) - RIE:CF4/CHF3/O2

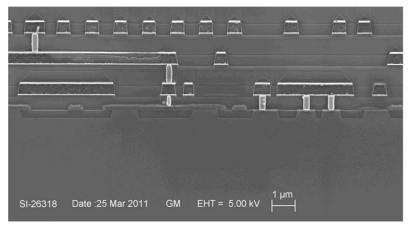


## **Delayering – Case study**

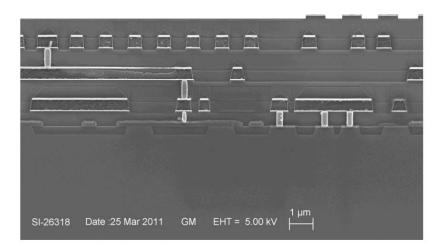




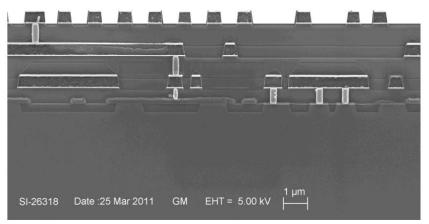
### DRY ETCH PASSIVATION (NITRIDE, OXIDE) - RIE:CF4/CHF3/O2







#### WET ETCH M4 - NaOH



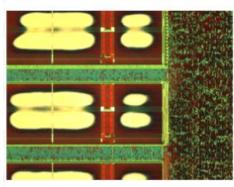
#### DRY ETCH IMD3 - RIE:CF4/CHF3/O2

### **F** Research

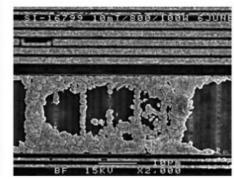
## Challenges

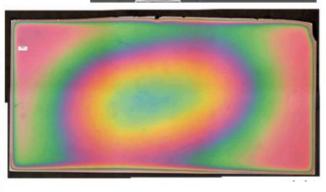


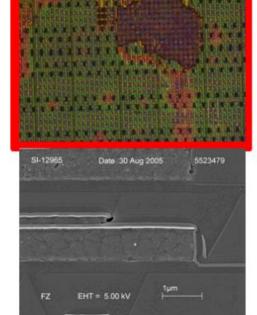
- Delamination
- Thin layers, half layers
- Planarity
- Material removal rates
  - Metal removal (grain boundaries)
- Pattern density
- Die size (thickness, length, width)
- Not enough parts



Research

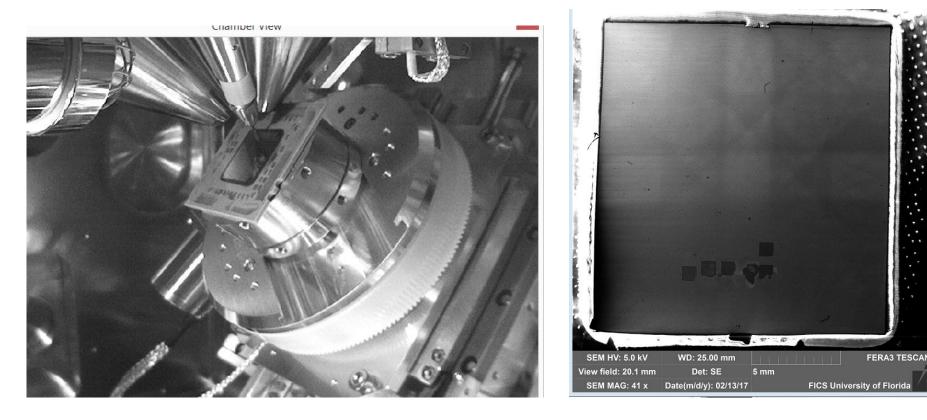






# **PFIB Delayering**







# **Readings and Videos**



- <u>https://www.youtube.com/watch?v=tnY7UVyaFiQ&list=PLe7niMUME</u> viOyD05aEA08IWVau\_sDEScH&index=11&t=0s
- <u>https://www.youtube.com/watch?v=oQzF-di-JQo</u>

