X-ray Tomography Applications for Electronics

Navid Asadi

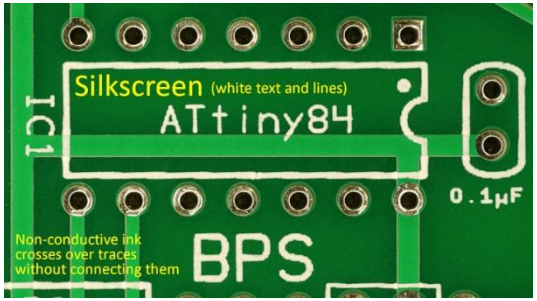
Physical Inspection and AttacKs on ElectronicS (PHIKS)

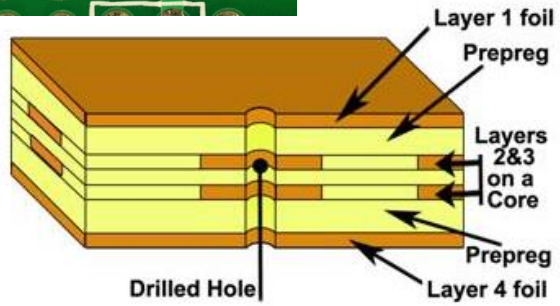
Printed Circuit Boards (PCB)

- PCBs and their applications:
  - ✓ Aerospace, Automotive , Medical, Telecommunication, Military, etc.

Tabtronics.net

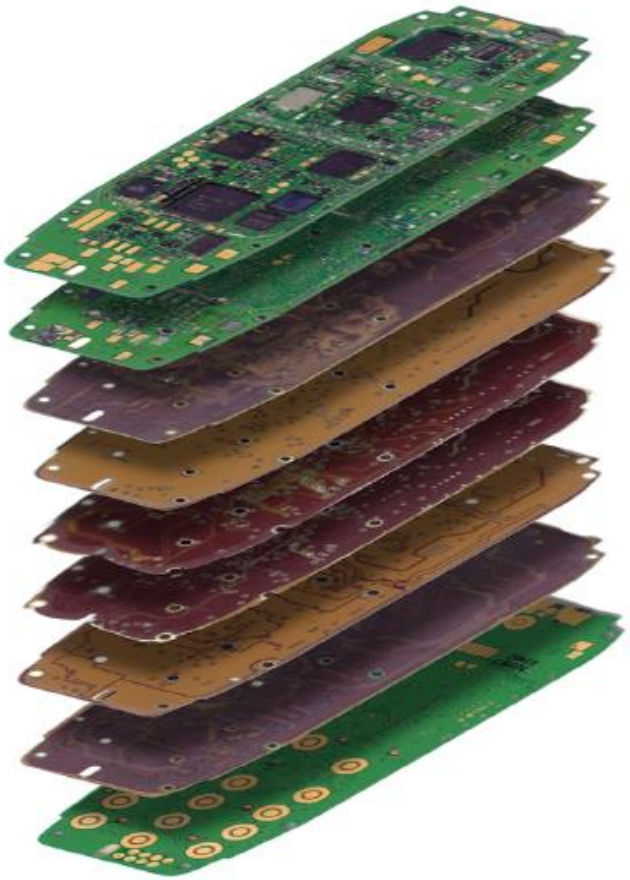
- PCB Composition
  - ✓ Conductive layers are laminated with non-conductive layers
  - ✓ PCB's surface is coated with solder mask
  - ✓ To identify the components, logos, test points, and parts of the PCB, silkscreen markings are often used





PCBs Reverse Engineering (RE)

- Primary purpose of PCB RE
  - ✓ Identify all components on the boa
    and the connections between them
- Goal
  - ✓ Removing exterior coatings
  - ✓ Accessing individual PCB layers



PCB RE Process

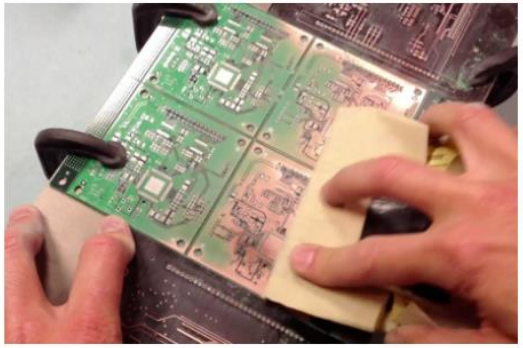
Destructive Methods

1. Solder mask removal
   - Goal is to remove the solder mask from the PCB
   - Expose the copper traces
2. Delayering
   - Access the inner copper layers of a multi-layer PCB by physical destructive methods.
3. Imaging
   - Digital imaging: save connection information of each layer before its removal

Non-destructive Method

1. Computerized Tomography (CT)
   - X-ray imaging method: series of 2D X-ray images are post-processed to create cross-sectional slices of the target object

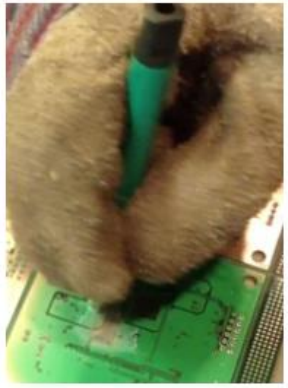
Solder Mask Removal

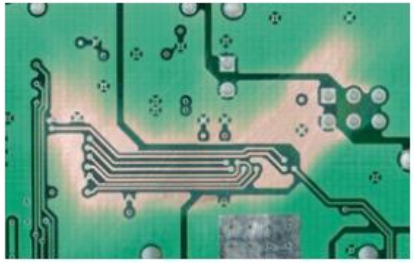


Using Sandpaper

Chemical

Laser





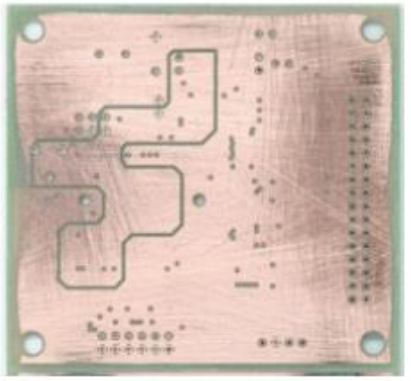
Using Fiberglass Scratch Brush

Abrasive Blasting

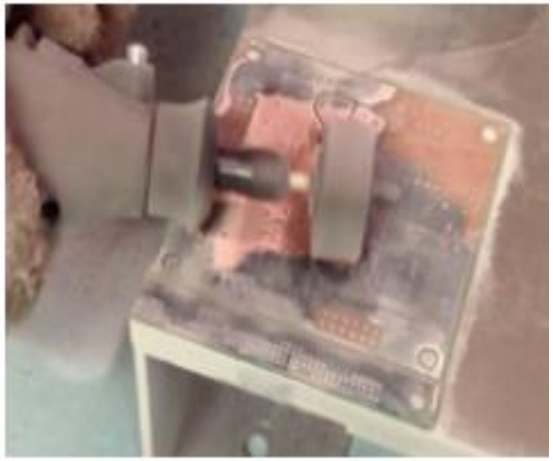
Joe Grand, USENIX Association, 2014.

Delayering

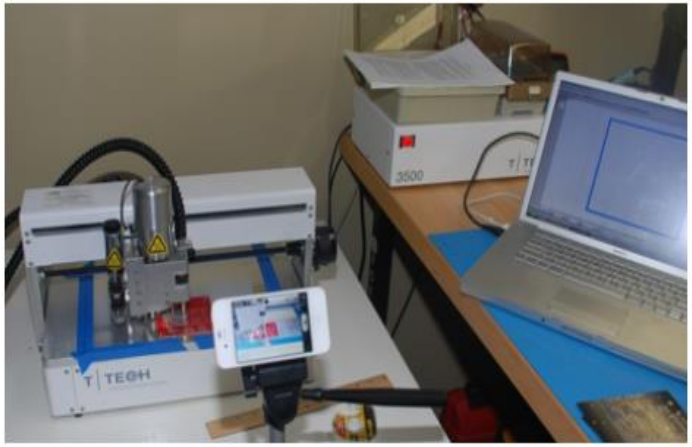
- Mechanical based delayering is a time consuming and labor intensive process for material removal

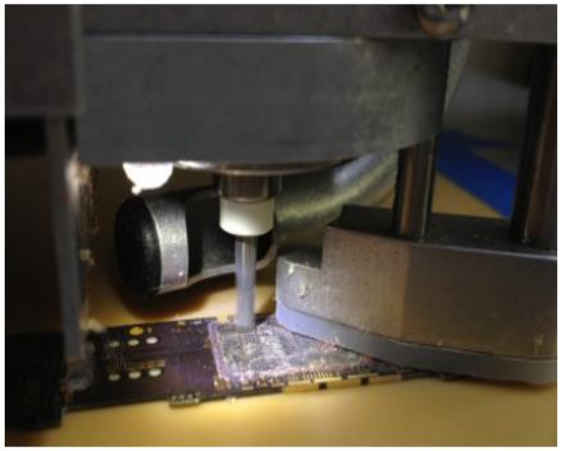


Sandpaper



Dremel Tool





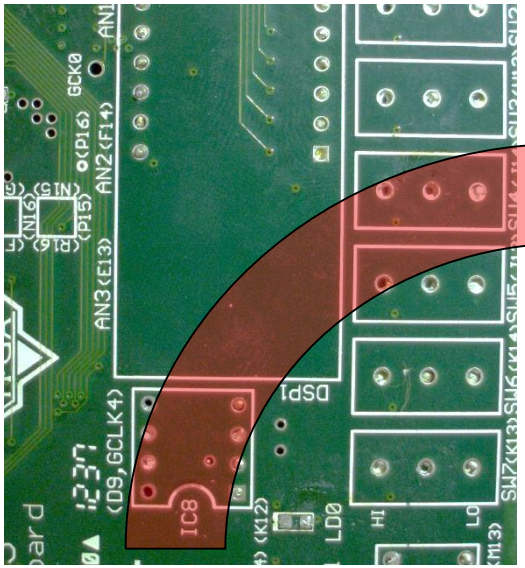
CNC (computer numerical control) Milling

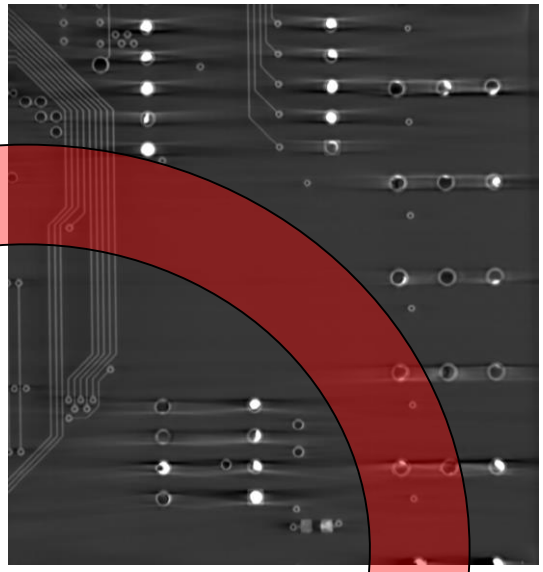
Joe Grand, USENIX Association, 2014.

Automated Non-destructive Imaging Using X-ray Tomography

Automated PCB RE Process

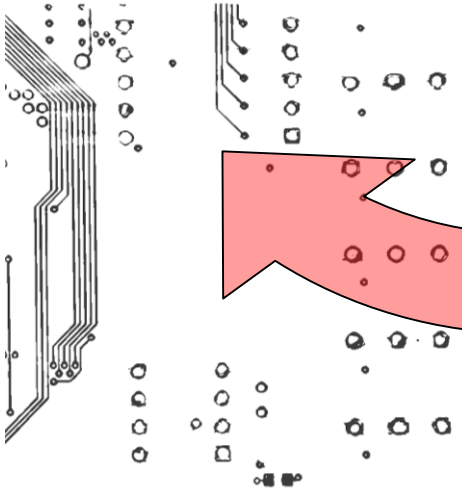
PCB

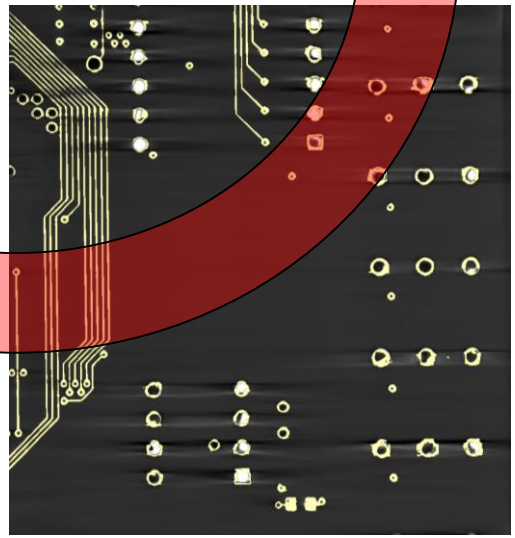




3D X-ray image

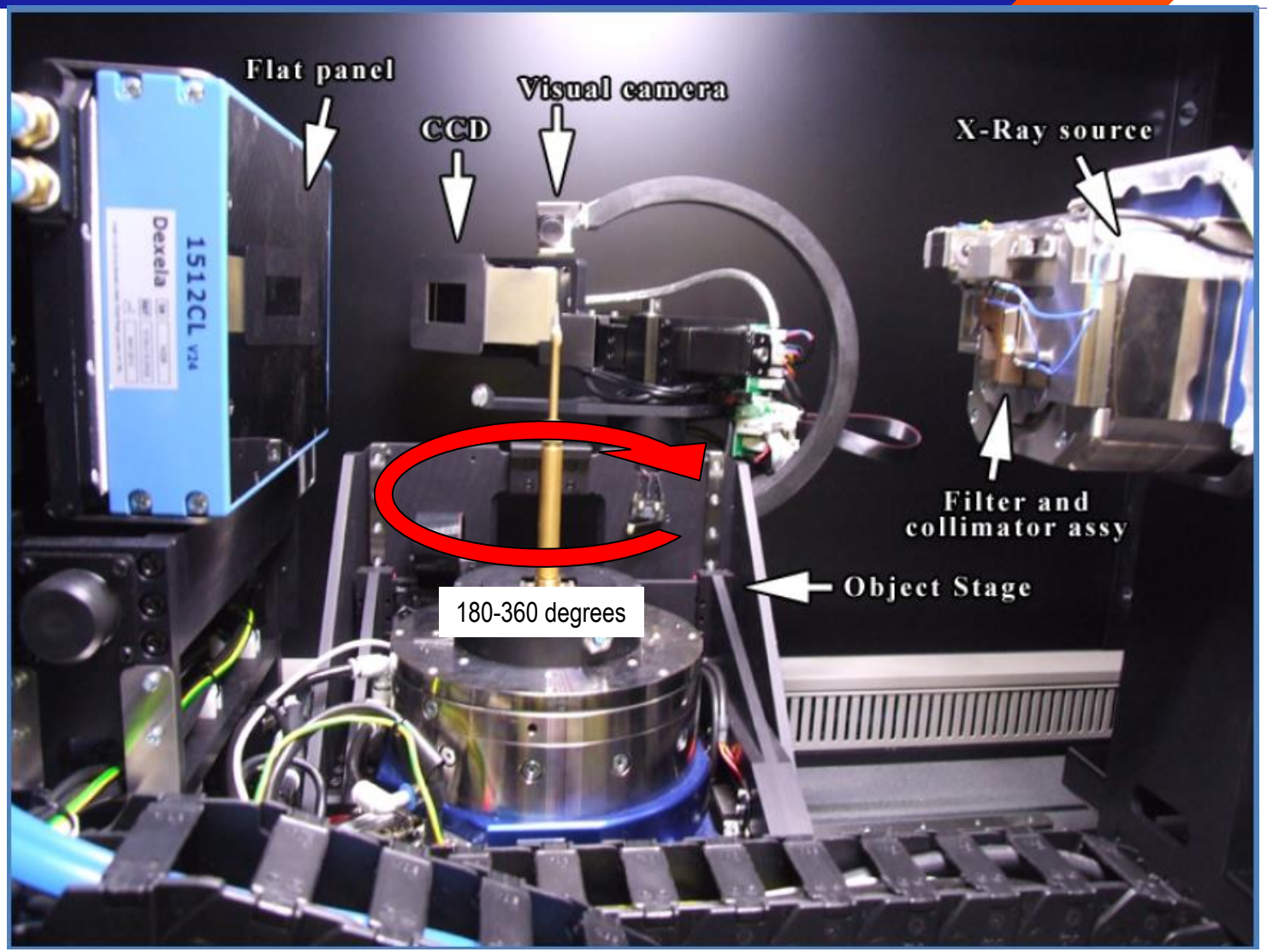
DXF or GERBER file



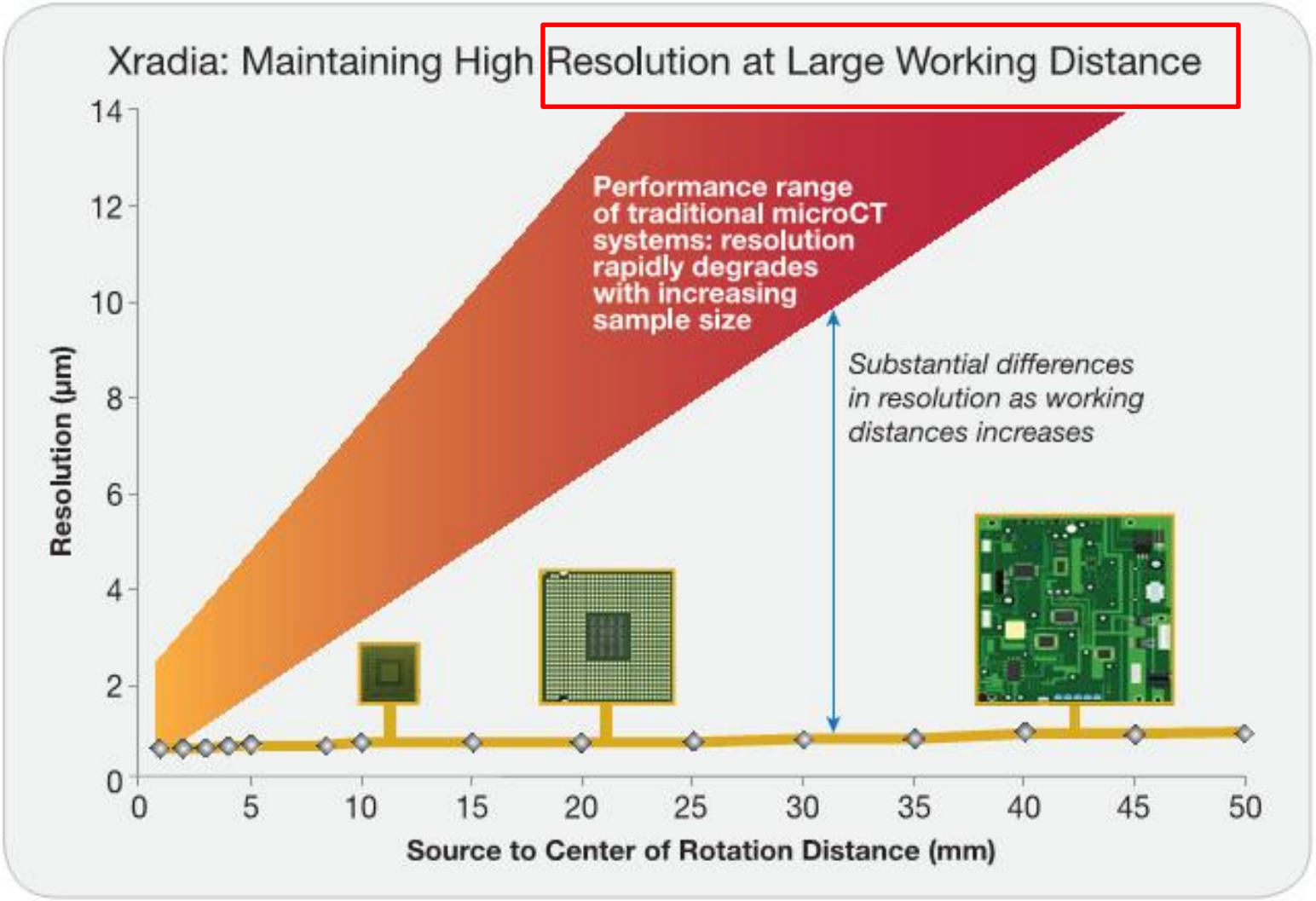


Segmented Image

X-ray Tomography of a Custom Board



Right Instrument for Our Purpose

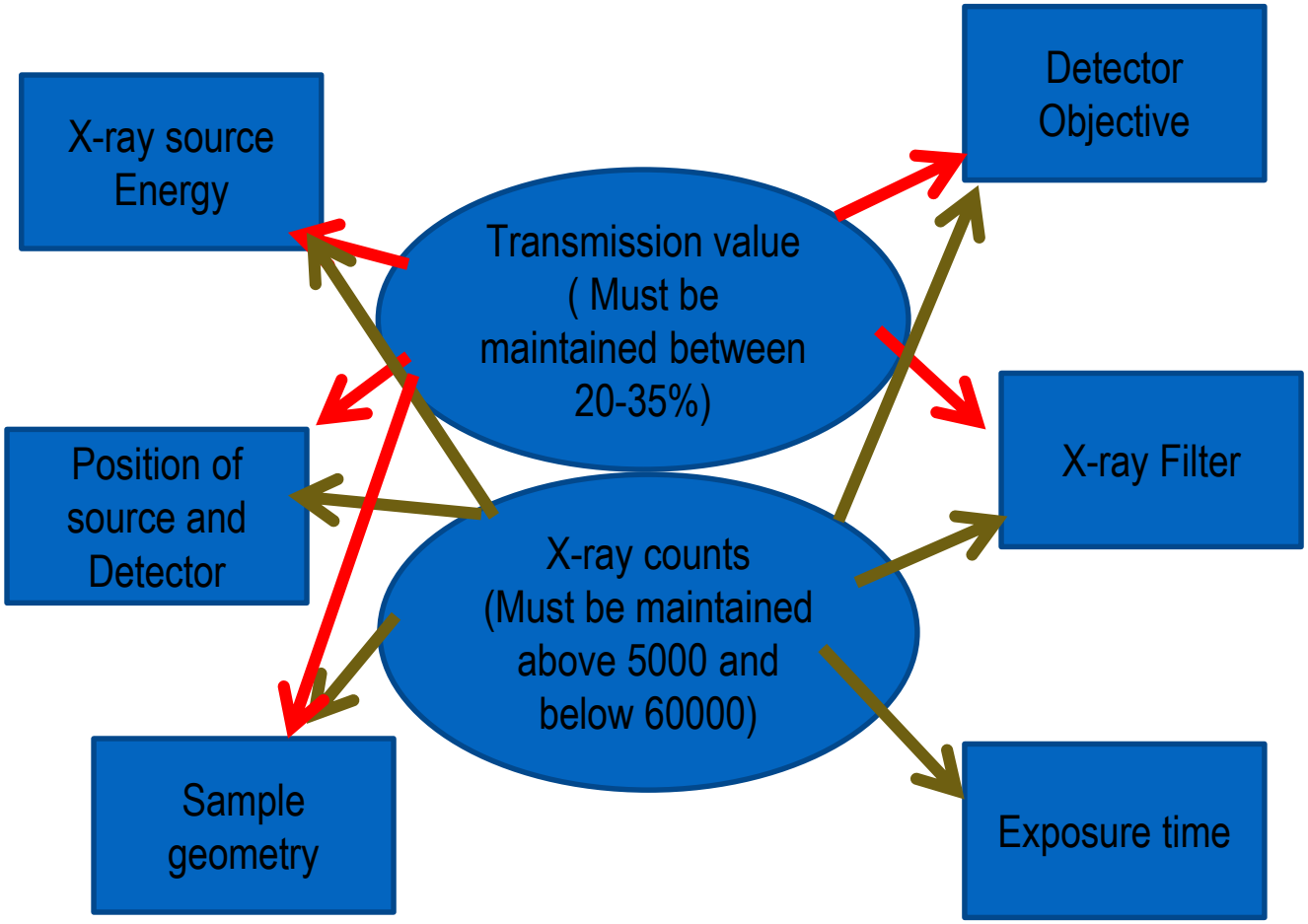


Acquisition Stage

Acquiring X-ray tomography is nontrivial

Tomography costs:

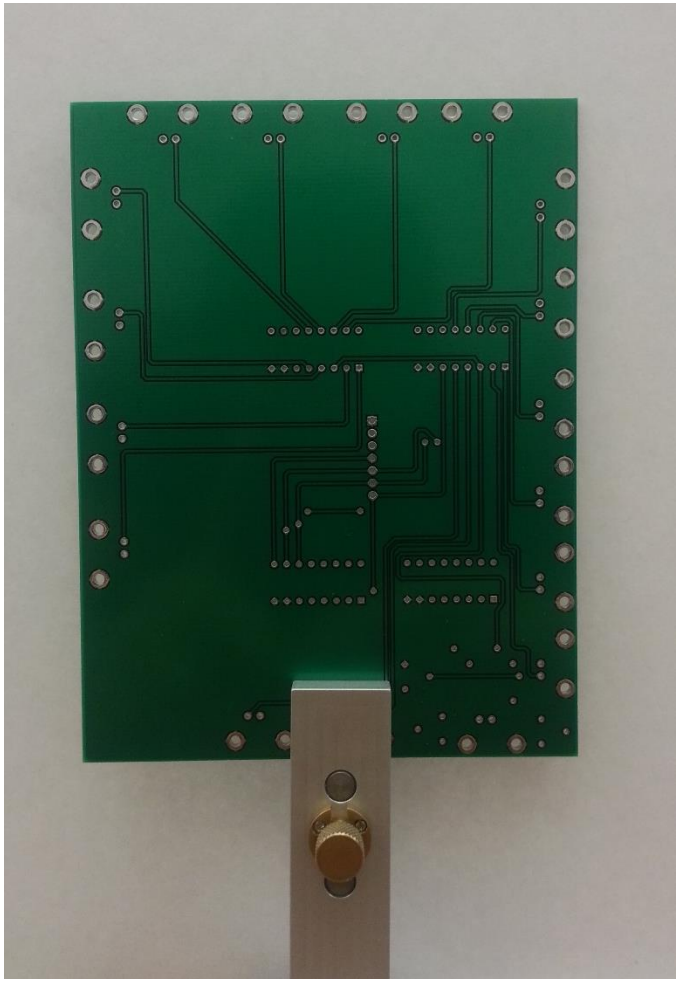
- More than 150 hours of scan have been done for about 50 scans.
- More than 100 hours for image reconstruction.
- Large file sizes, about 2GB for each tomography.



PCB Tomography

- X-ray tomography parameters have been optimized after several rounds of tests to better capture the intermediate layers structure

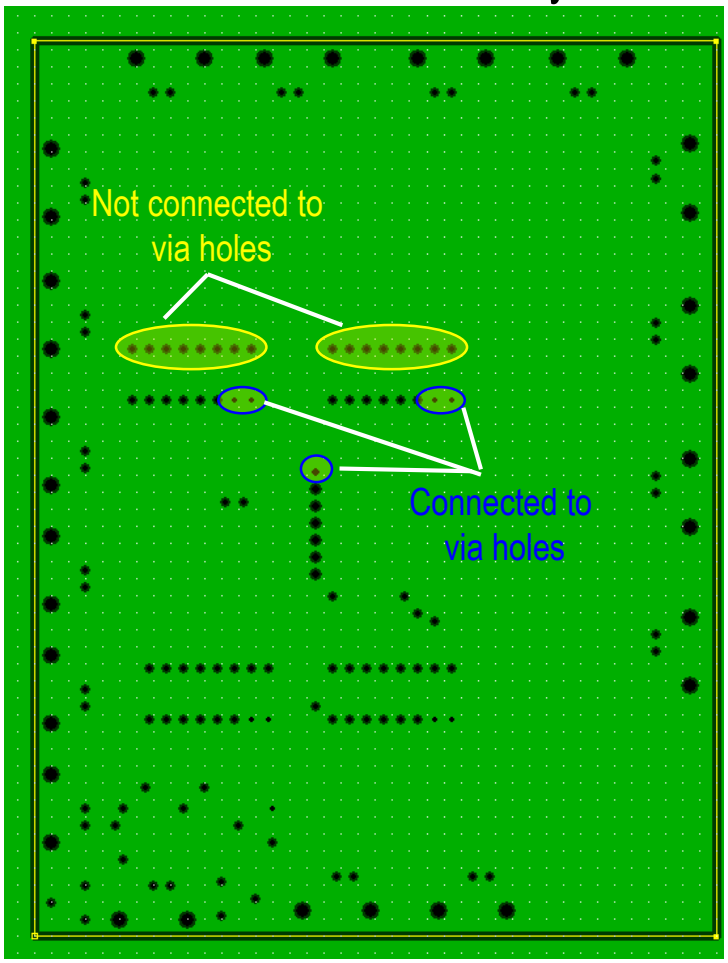
- Four layer PCB Including two intermediate layers:
  - Power layer
  - Ground layer
  - Two side layers



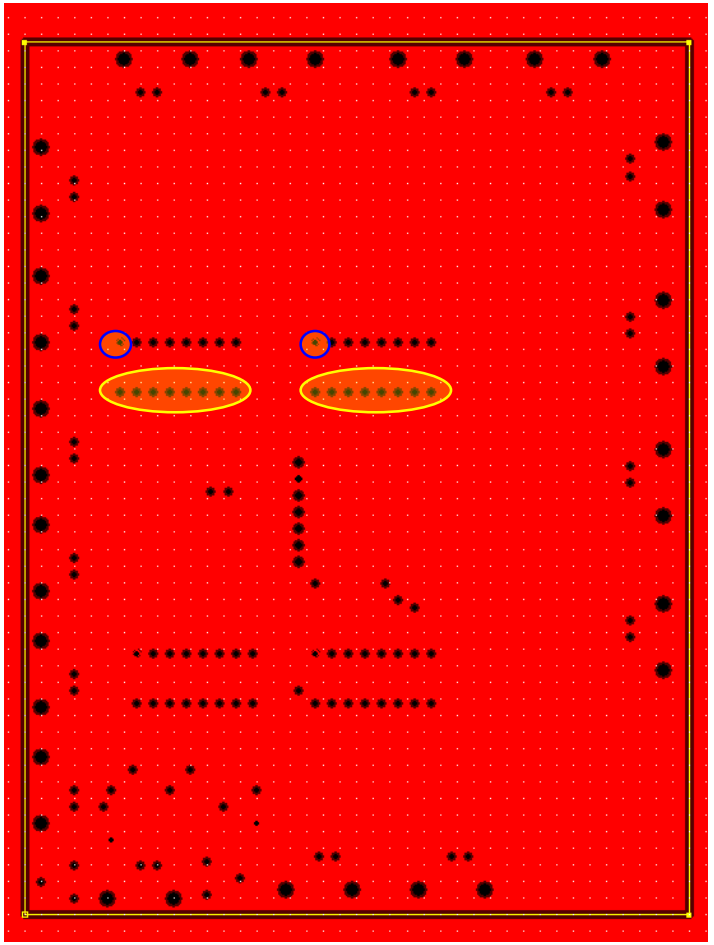
PCB mounted in sample holder

Intermediate Layer's layout

Power Intermediate layer



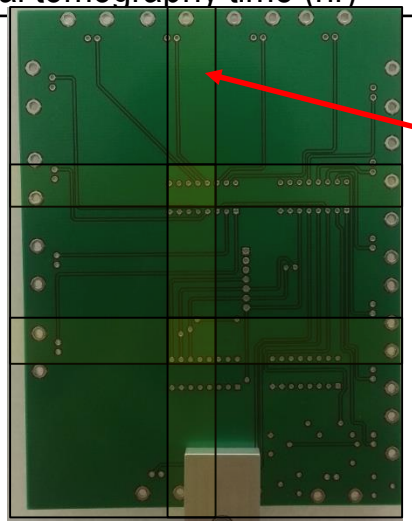
Ground Intermediate layer



Optimized Tomography Parameters

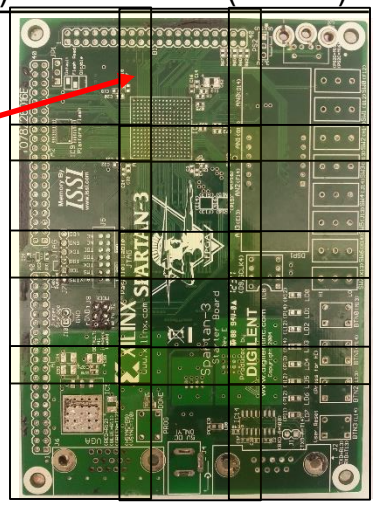
- **Multiple scans are taken to cover the complete board.**
- **20% overlap is needed to provide correlation information for stitching in the reconstruction step**
- **One time set up is required to run all the scans.**

Tomography parameters	Custom board	Spartan 3
Pixel size (μm)	49.2	47.9
Window size (mm)	49.5	48.5
Detector	0.4X	0.4X
Source distance (mm)	204.2	200.0
Detector distance (mm)	80.1	86.0
PCB aspect ratio	10-0.3	14-1.5
Exposure time (s)	1.2-7.2	1.5-9
Number of projections	1601	1601
Number of scanned areas	6	12
Total tomography time (hr)	9 (6*1.5)	18 (12*1.5)



Costume board

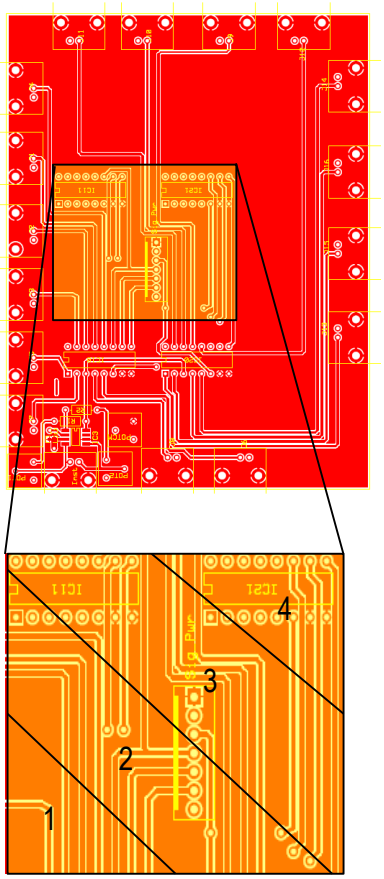
Overlapped areas

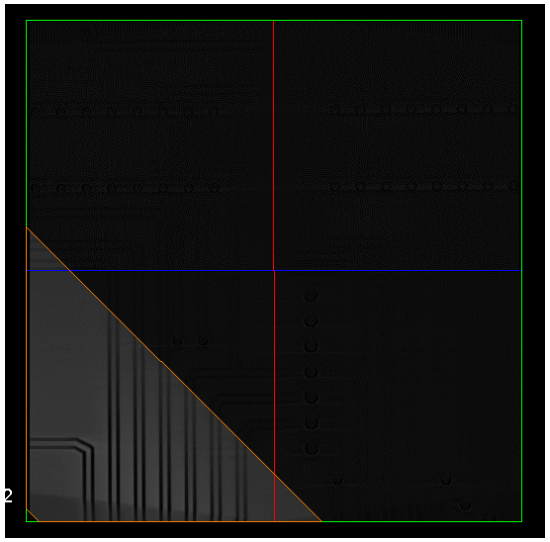


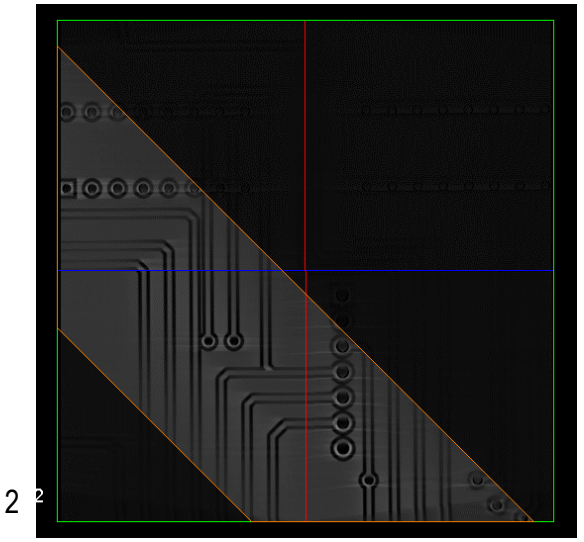
Spartan 3

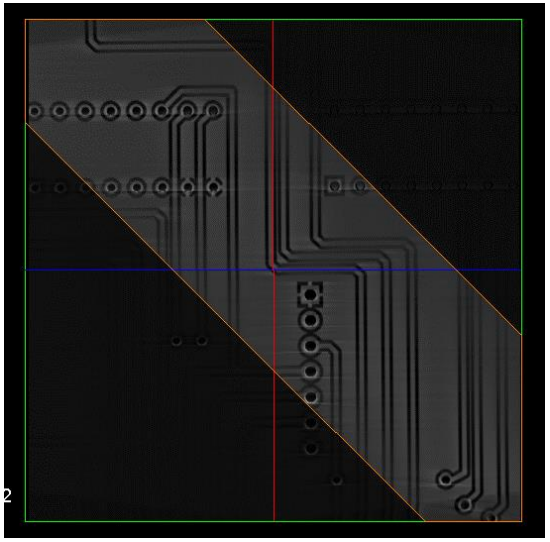
Layer #1

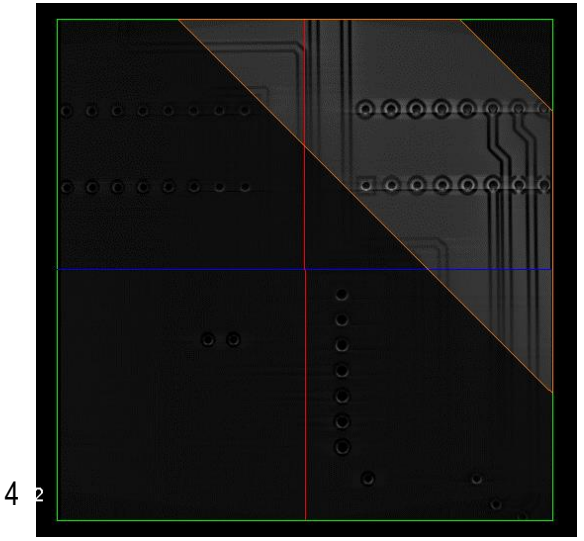
Imaged Area





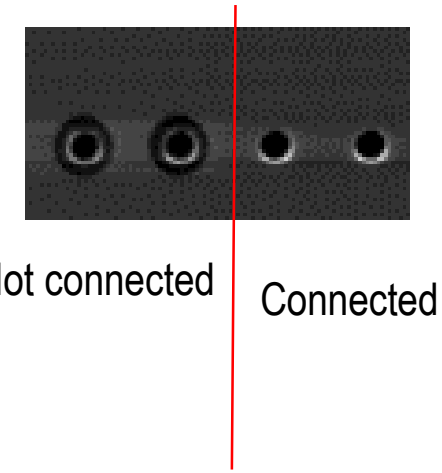


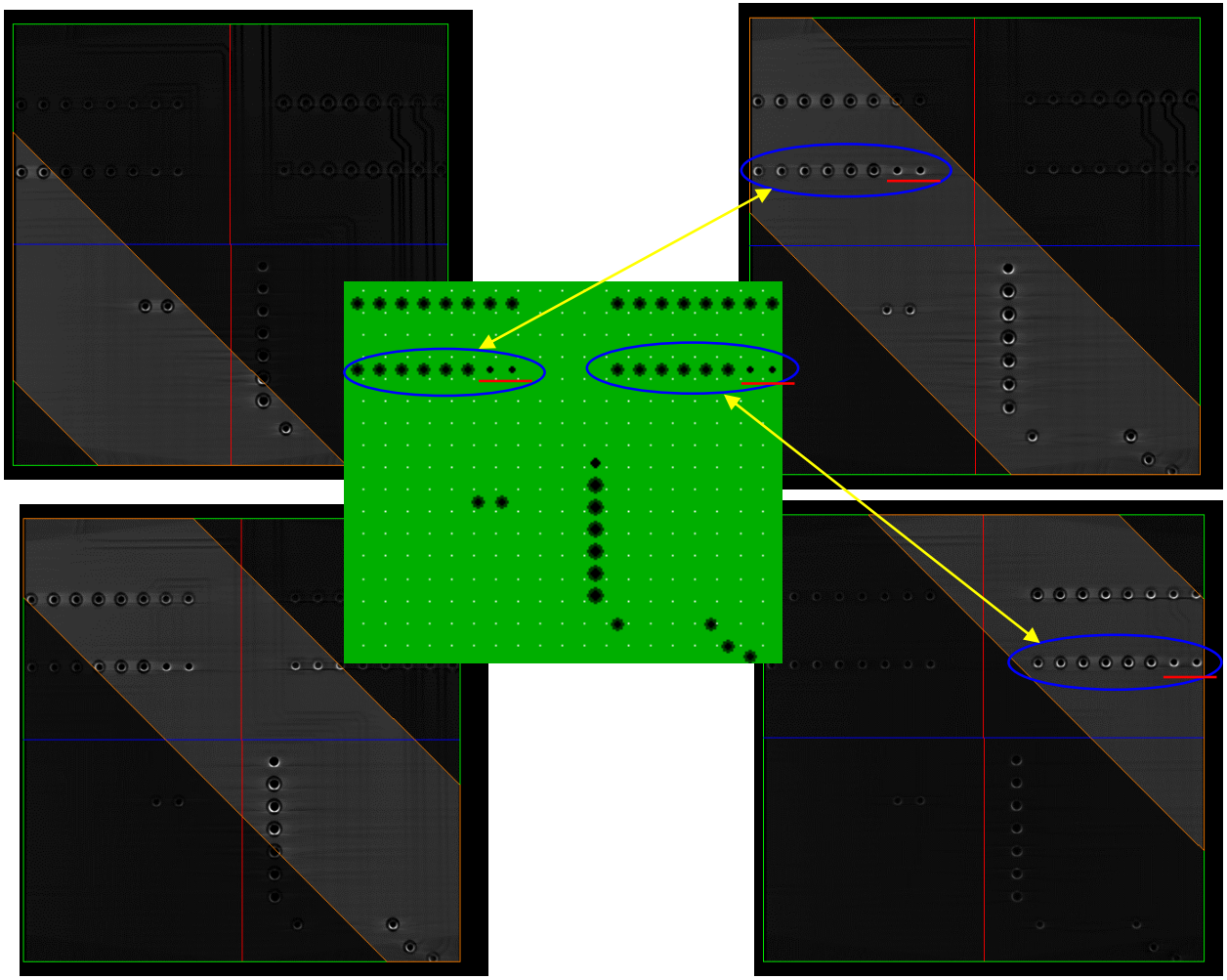




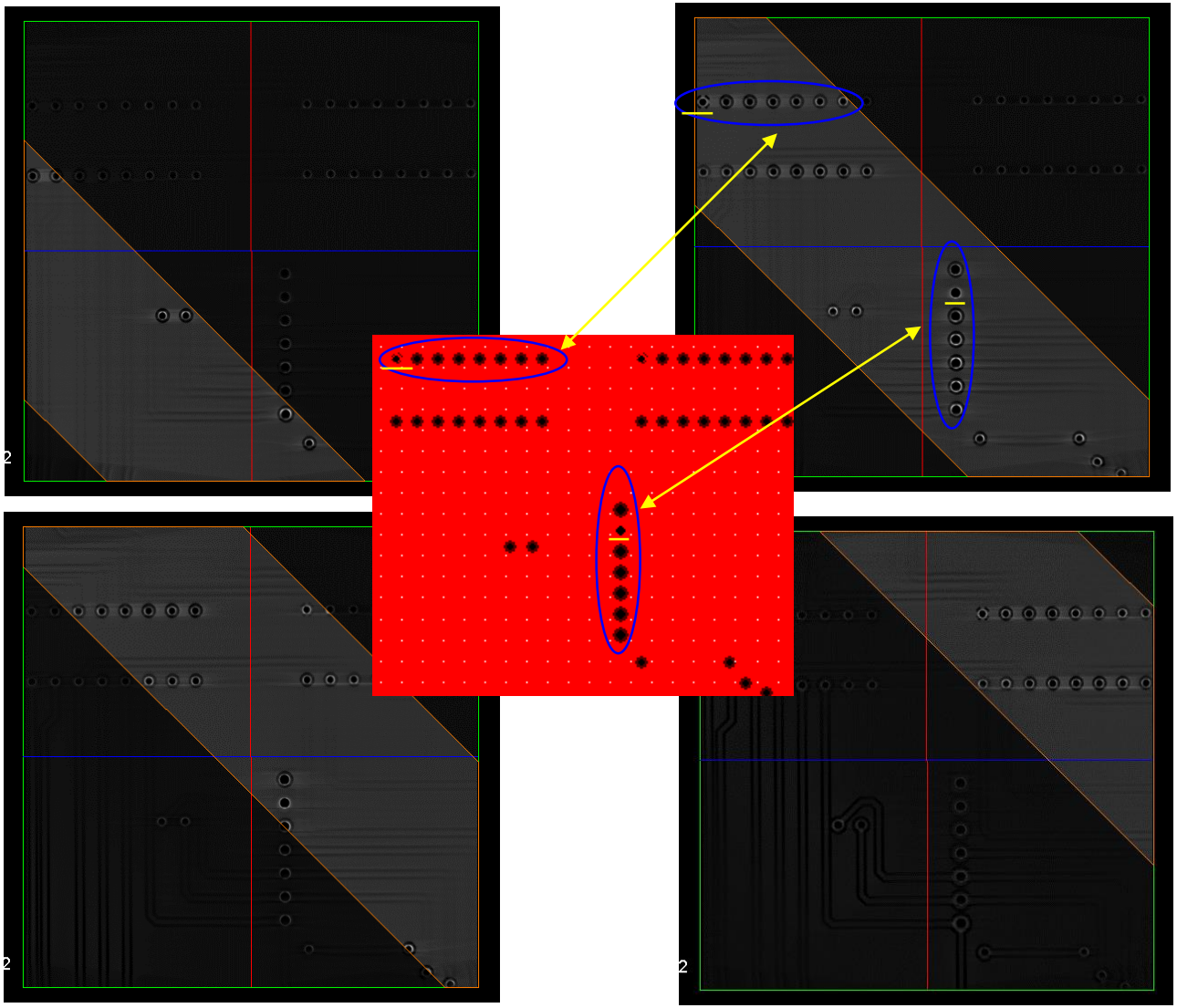
Layer #2, Power Layer

Connected and not connected via holes captured with X-ray

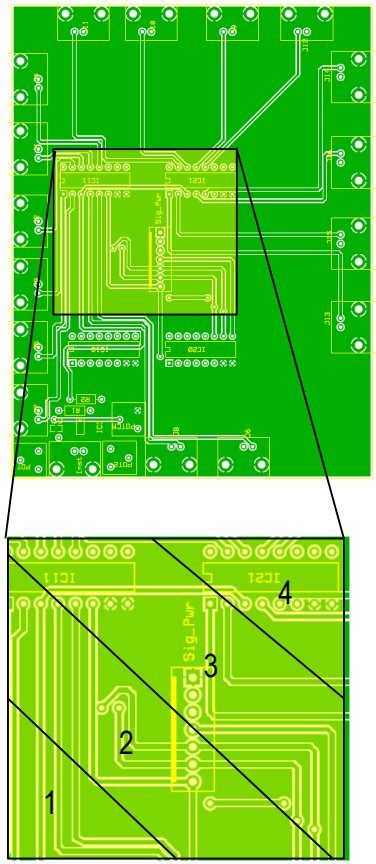


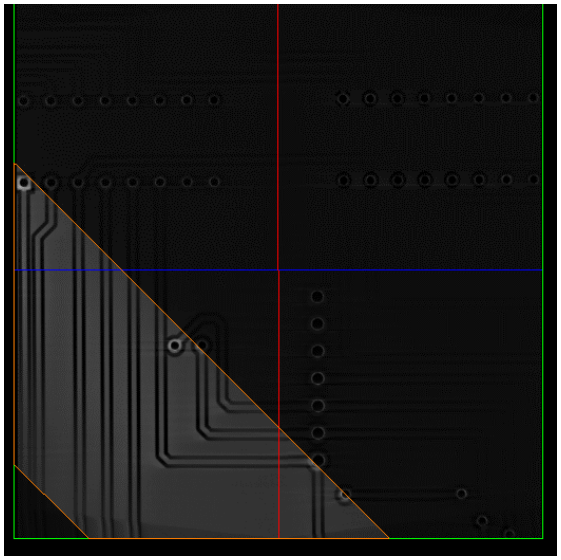


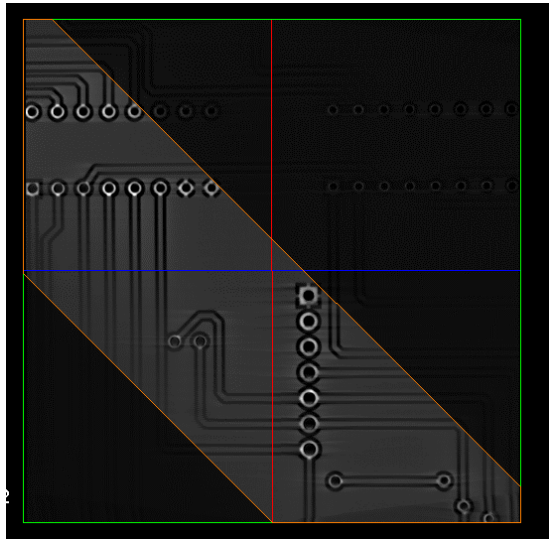
Layer #3, Ground Layer

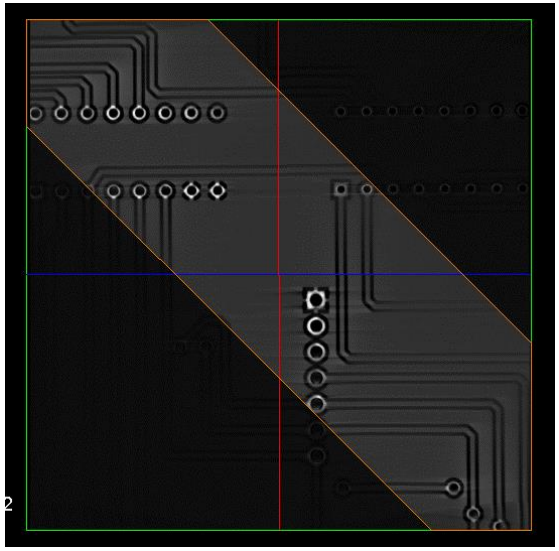


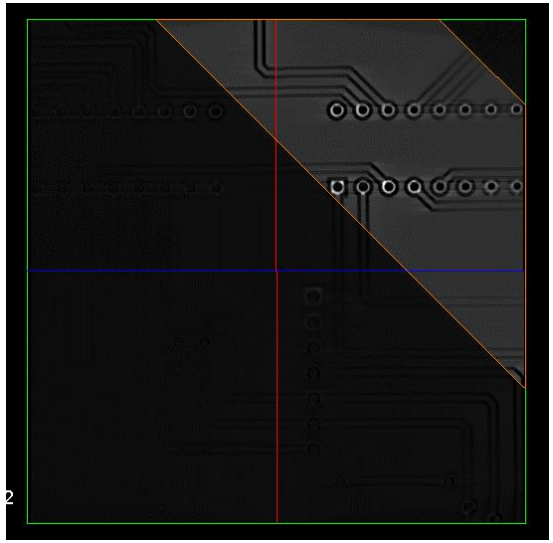
Layer #4, Bottom



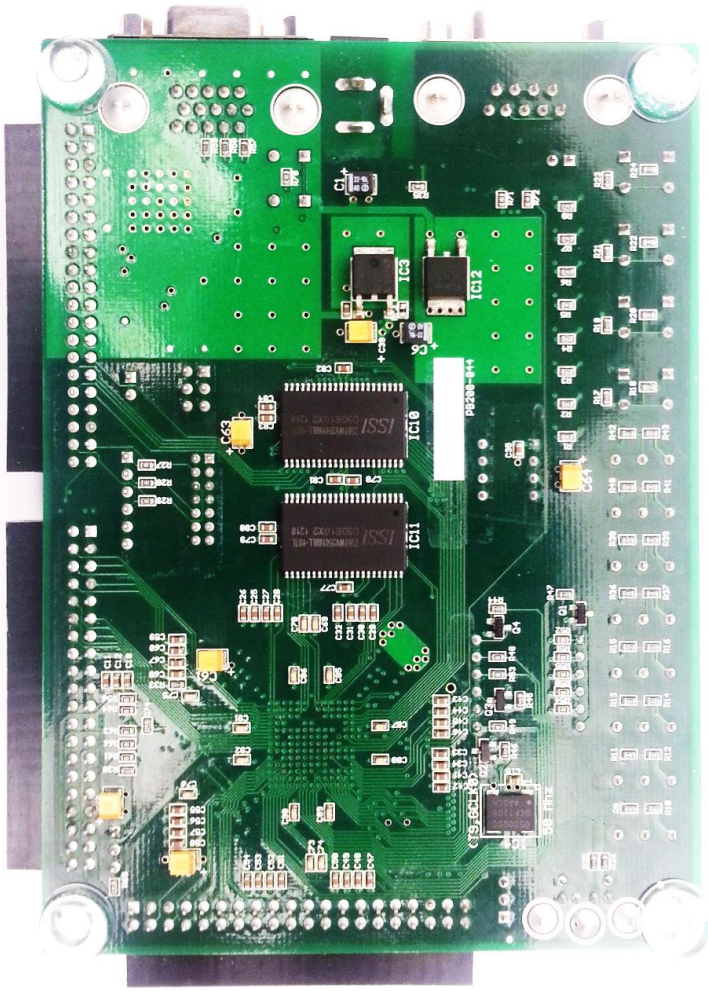








RE of a Commercial PCB

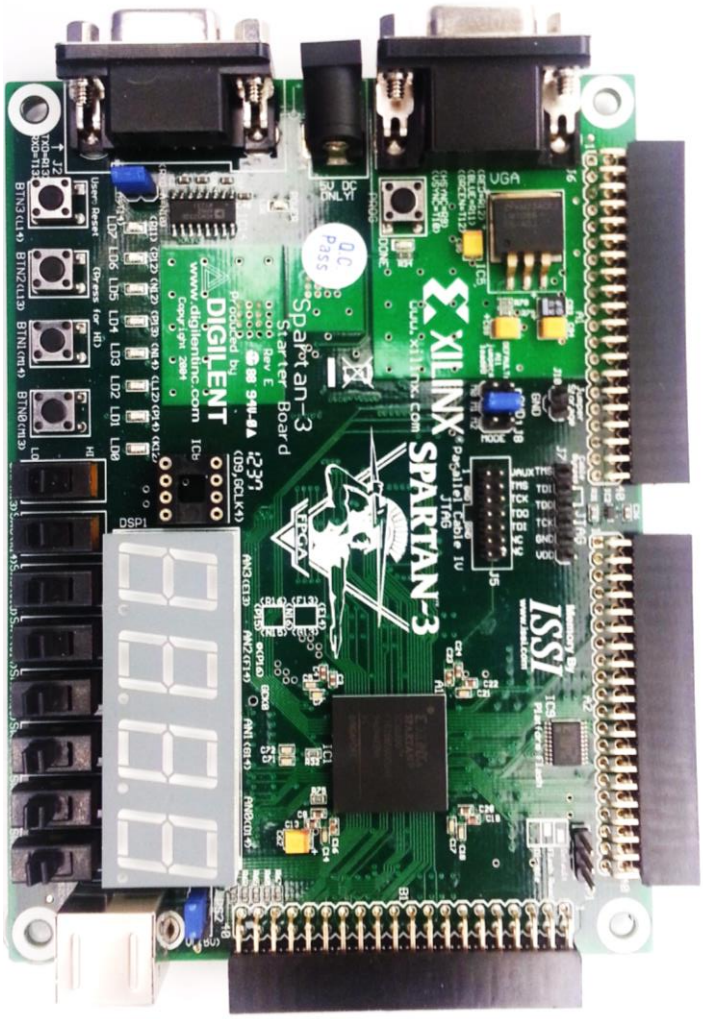


Xilinx Spartan 3

6 layers PCB
2 layers for ground and power

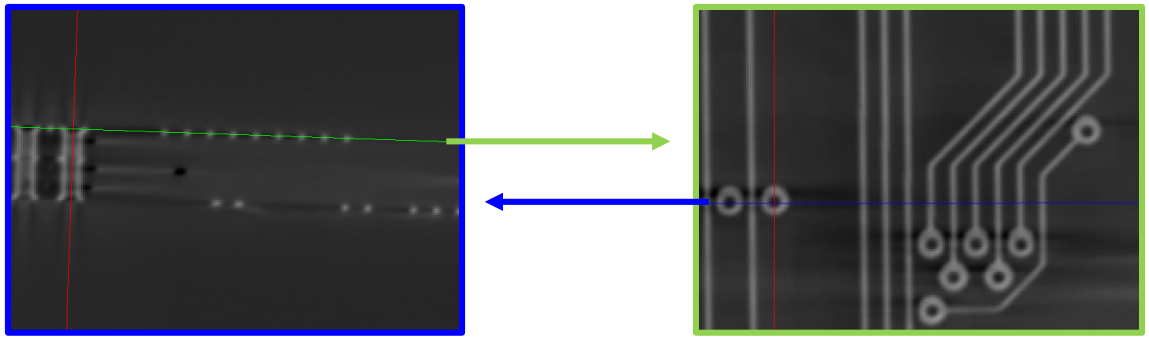
Front view →

← Back view

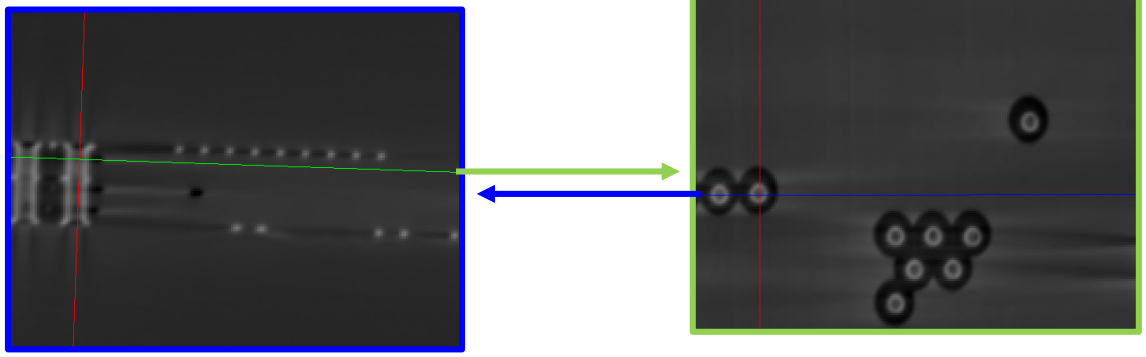


Spartan 3 Layers 1-3

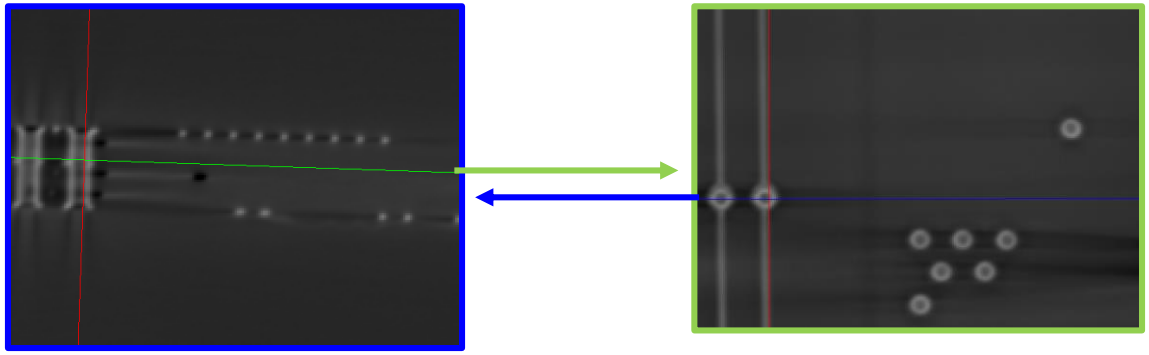
Layer 1



Layer 2

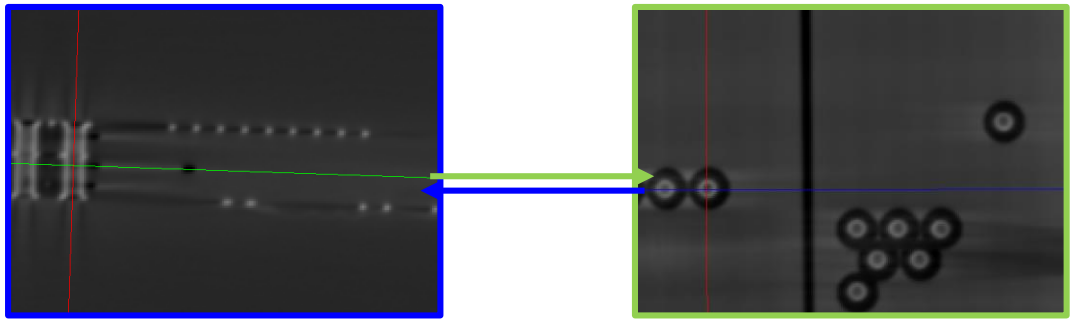


Layer 3

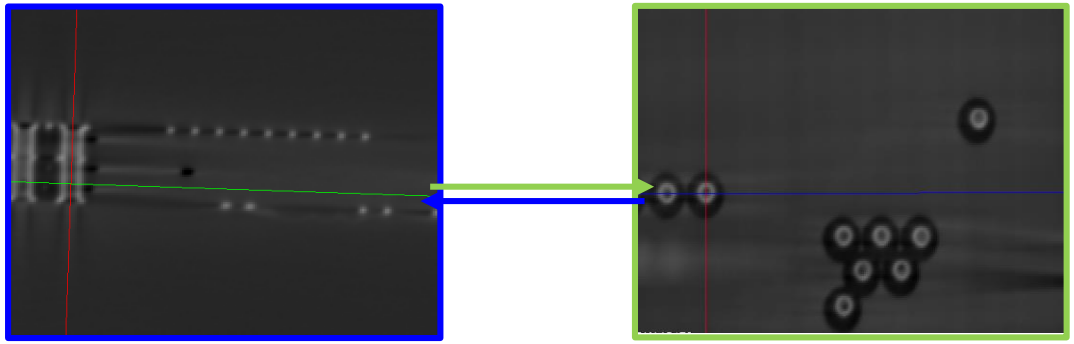


Spartan 3 Layers 4-6

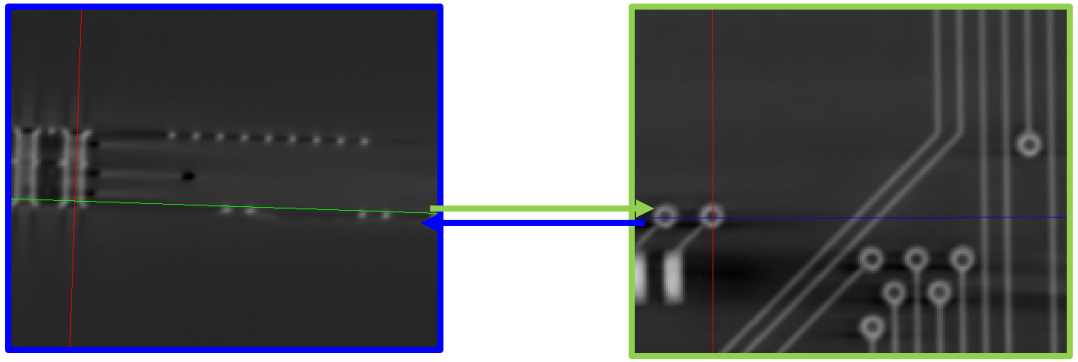
Layer 4



Layer 5



Layer 6



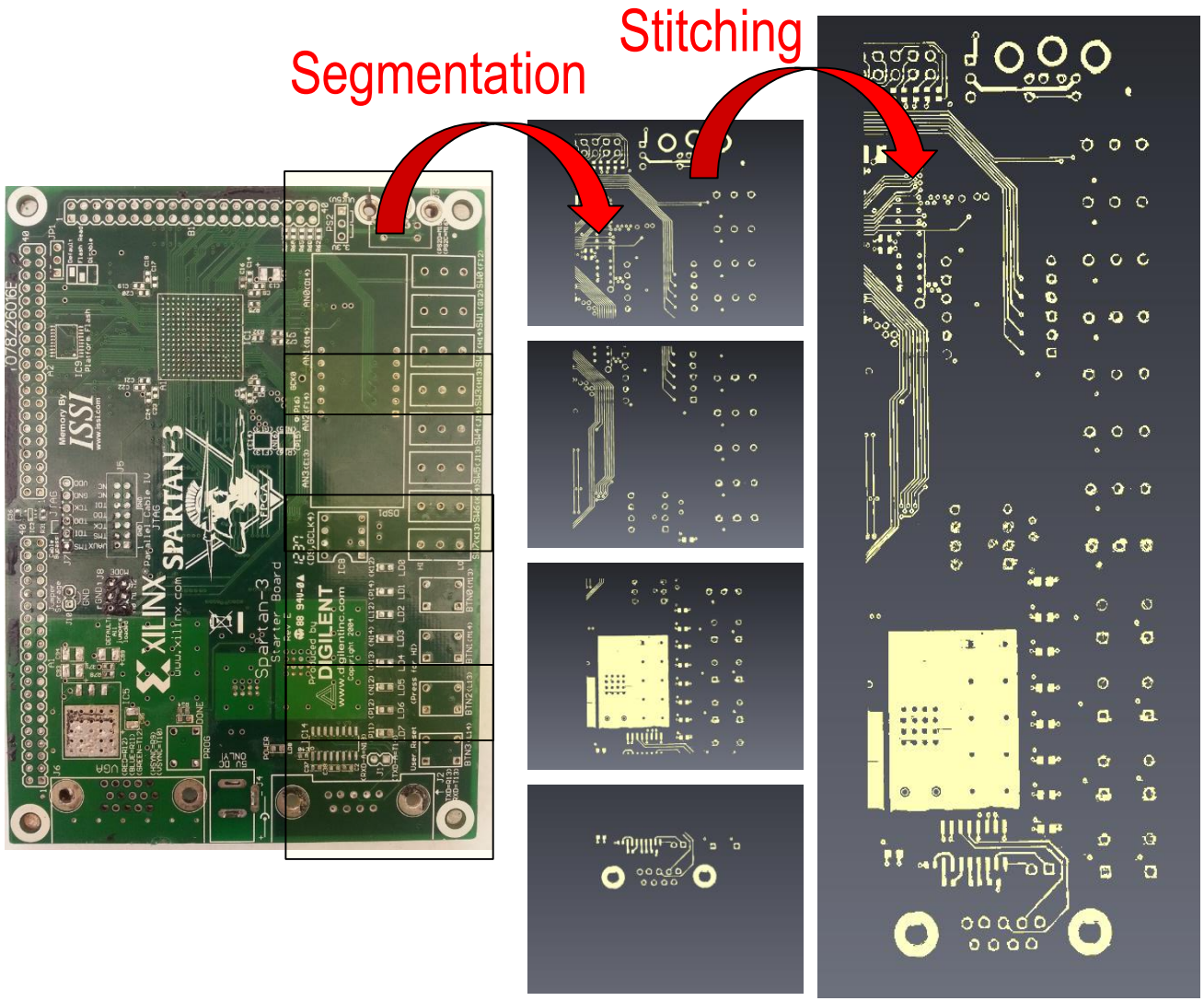
Generating CAD Files

Segmentation:

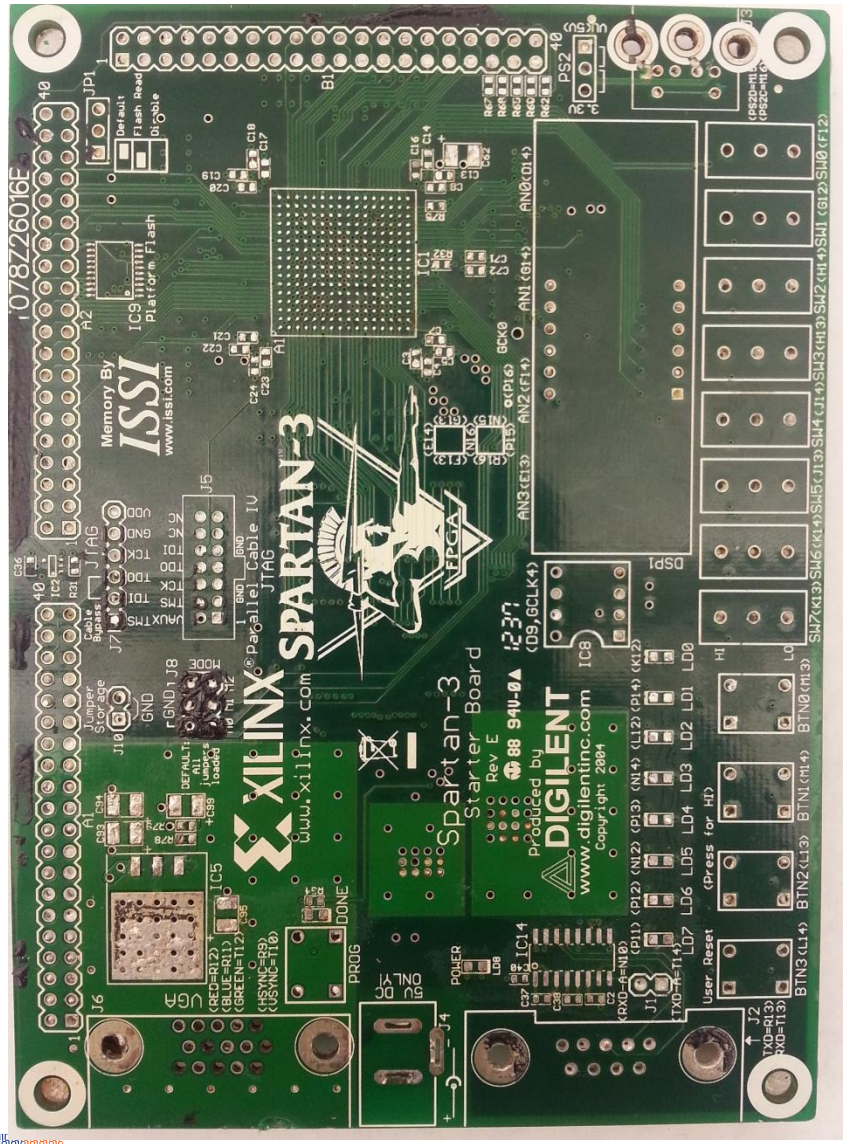
1. *Smooth* images to minimize noise
2. *Assigning material* to each pixel based on pixel contrast for segmentation

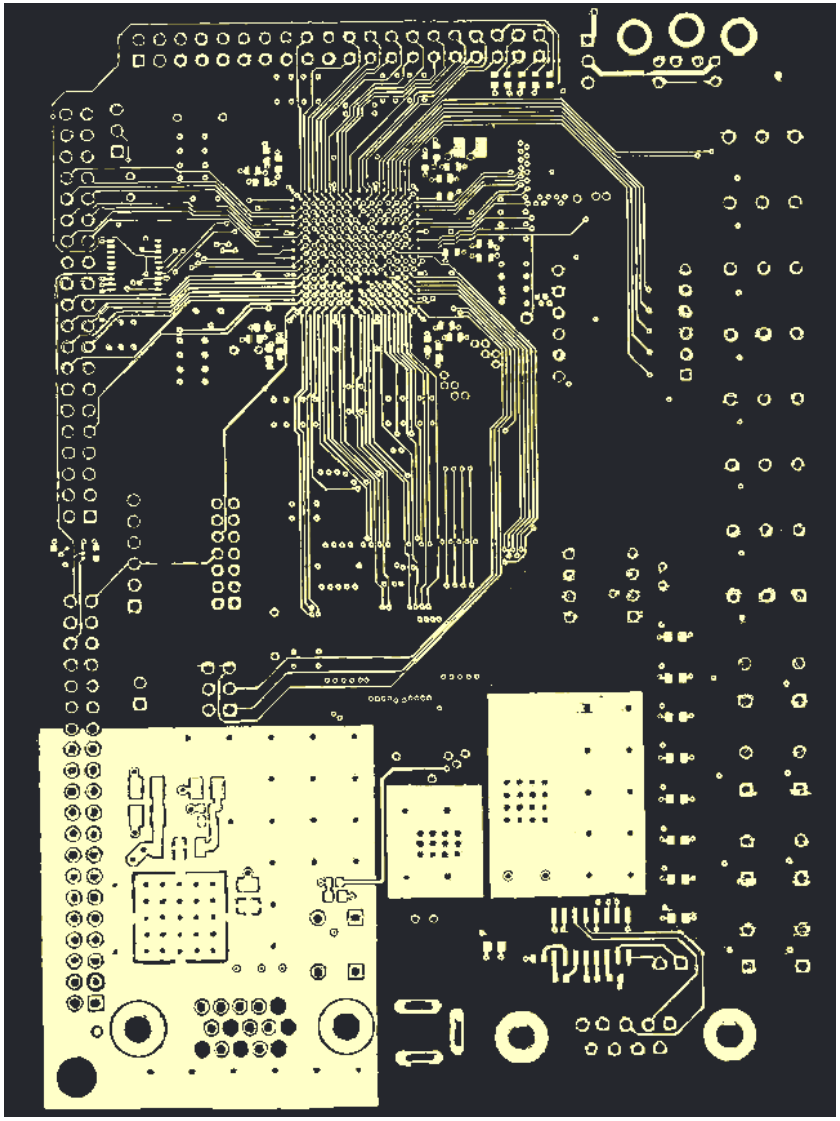
Stitching:

- Using the features in the overlapped region to *correlate* two images and *merge*.



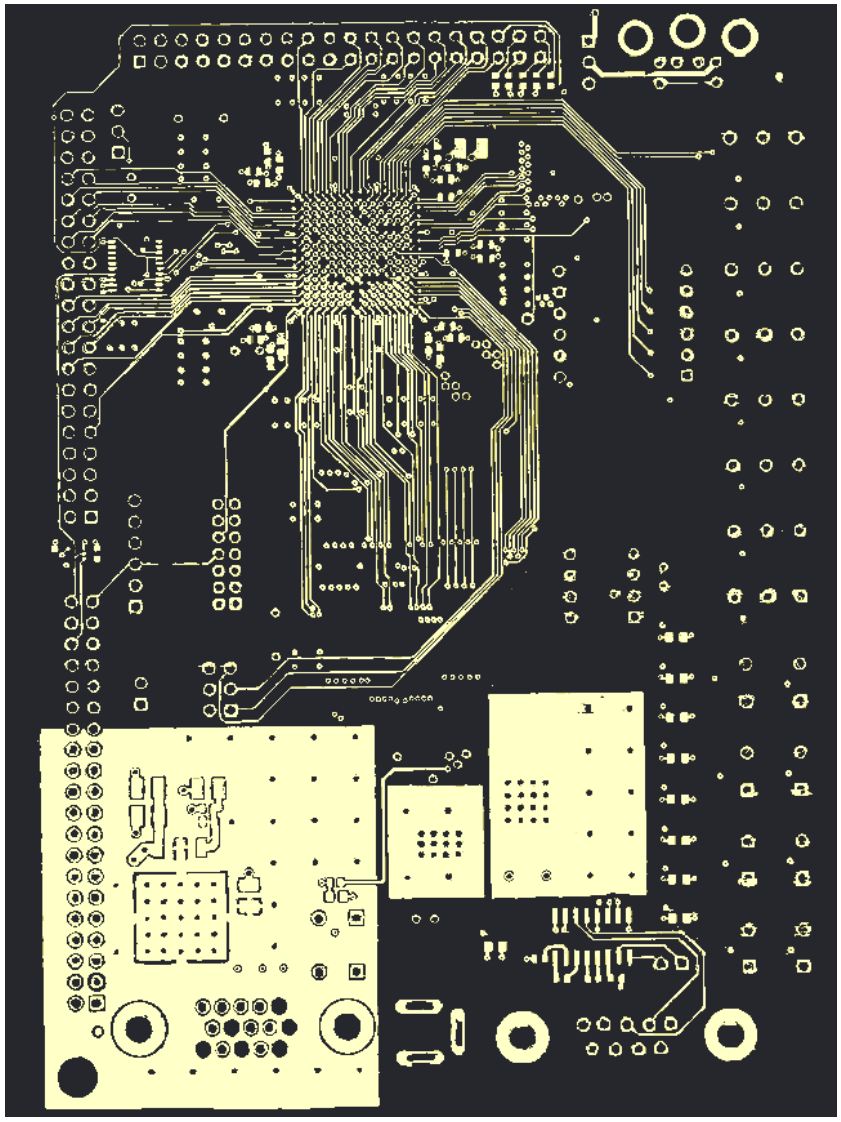
Complete Layer Segmented





Segmented Layers 1-6

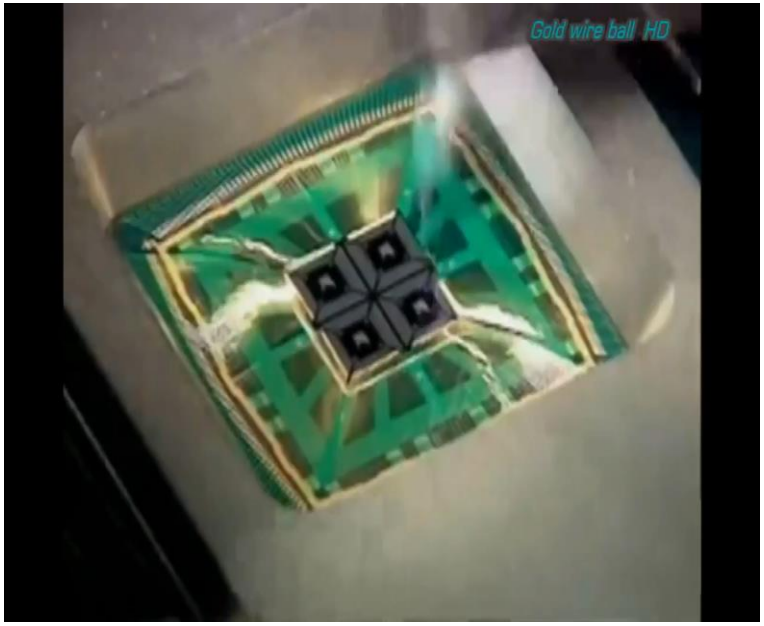
Layer 1

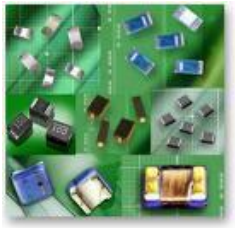


Virtual Bond Pull and Ball Shear Analysis

Bond Wire Quality and Assurance

- 95% of integrated circuits use wire bonding (gold, aluminum, etc.)
- Higher grade microelectronics require better standards for harsh environment
- Quality and assurance requires monitoring breaking force





Chip Package Decapsulation

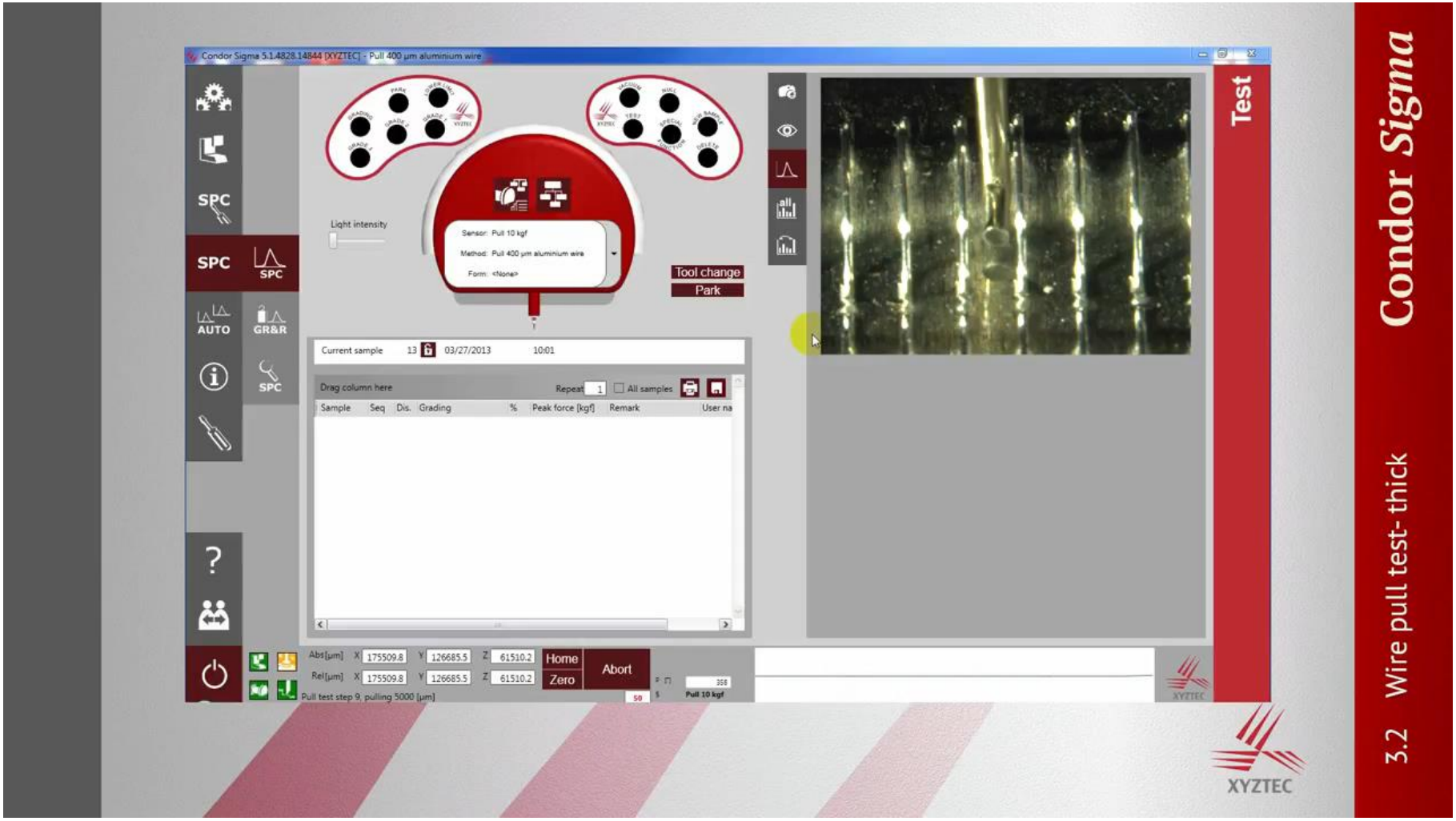
- Manual grinding and polishing
- Chemical decapsulation
- Abrasive blasting
- Plasma Etching
- Laser decapsulation

Methods above require expert skill, and cost a lot of time and money

VarioEdit Laser Assisted Chemical Etching tool

- Price : $750K
- Can performs local decapsulation using laser

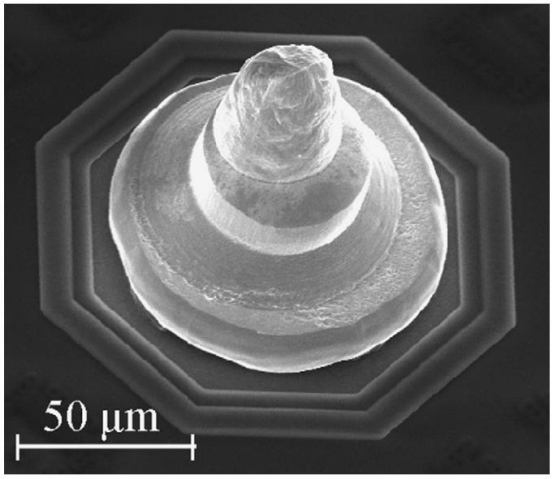
Destructive Bond Wire Pull Test

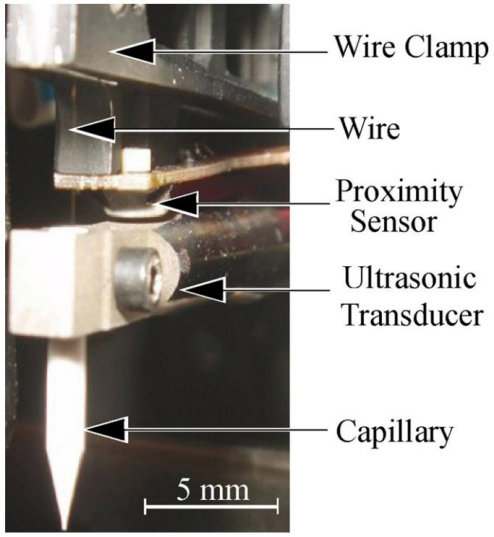


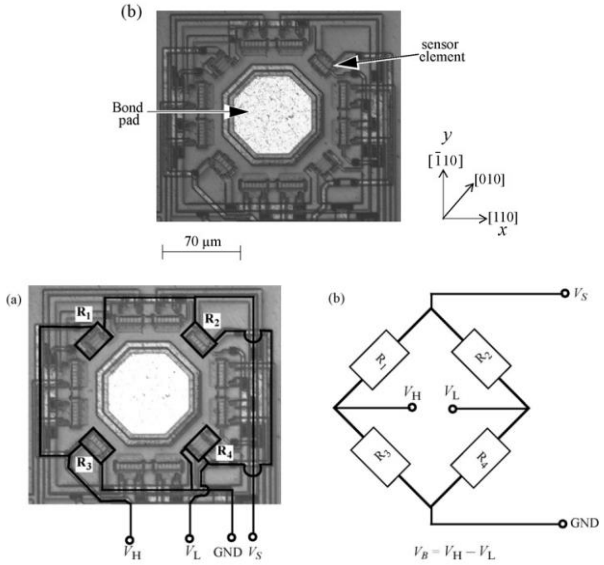
Online Force Measurement

1. **Piezoresistive microsensor** integrated next to the bonding pad
- The Au wire breaks at the heat-affected zone (HAZ) next to the ball bond
- Microsensor signal is highly sensitive to ball and pad geometry, values of the piezoresistive coefficients, and the z-location of the microsensor under the bonding pad

2. **Proximity sensor** attached to the wire clamp of the bonding machine
- A displacement sensor works on the eddy current principle to sense proximity of conductive materials







Aashish Shah et. Al. 2008

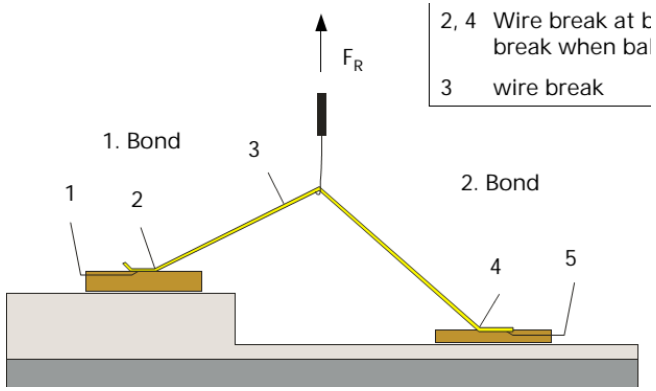
Actual Mechanical Testing

Failure modes:

1, 5 Bond lift off from pad metallization (lift off)

2, 4 Wire break at bond (heelcrack or neck break when ball/wedge bonding)

3 wire break

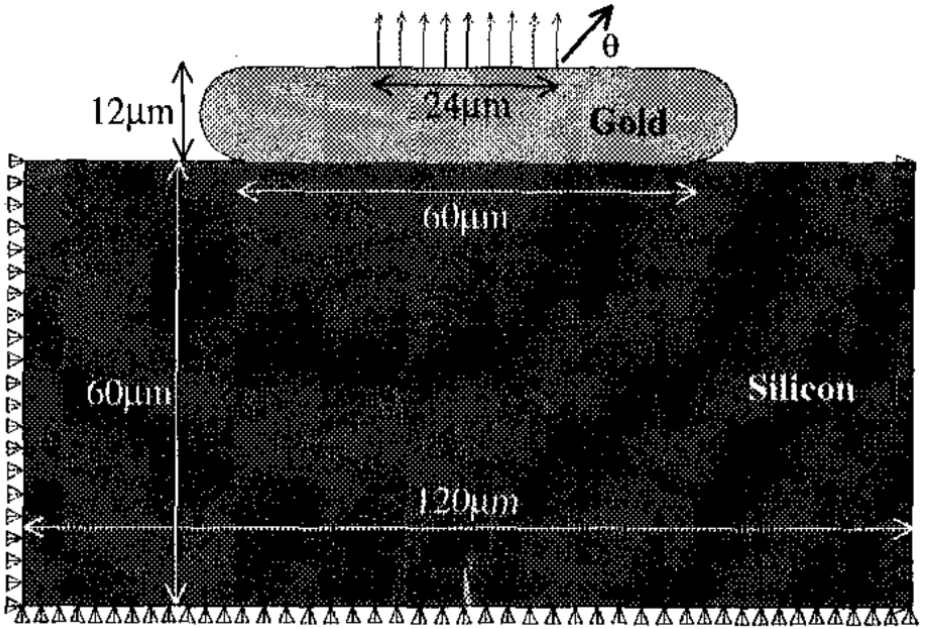


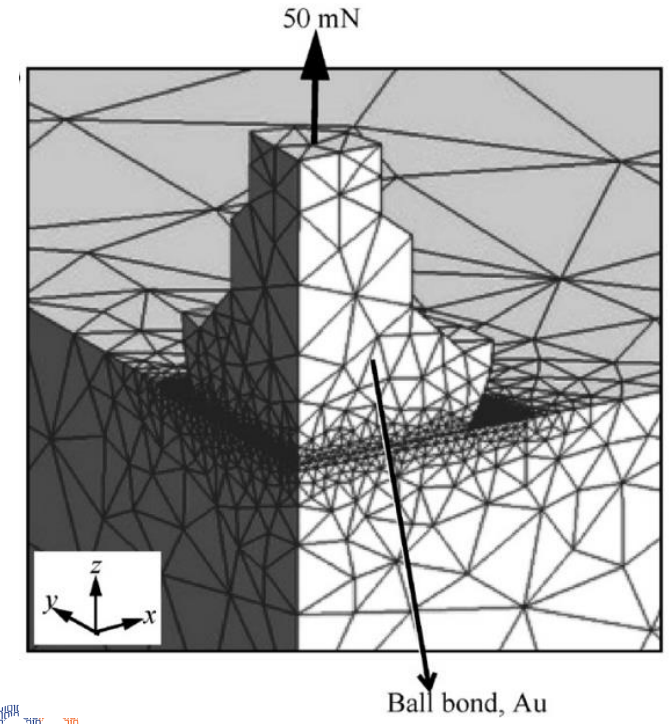
Disadvantages

1. Package should be entirely or at least partially removed
2. Each wire can be used for only one test
3. Durability and Fatigue Analyses require long testing times
4. The effect of mechanical load is exerted on one wire at a time

FE Simulation Challenges

- Not necessarily representative of the real geometry and structure of wires
- Modelling efforts have utilized 2D SEM images





Geometry Simplification is inevitable while modelling a 3D structure

3D Information Advantage

Tomography parameters for microchips

	TL 145406N	AD7512DIJN
Magnification	35.94	37.98
Voxel size (µm)	5.56	5.26
Focus-Object-Distance (mm)	22.39	21.2
Focus-Detector-Distance (mm)	805.22	805.22
Number of projections	1200	1200
Source voltage (kV)	200	200
Source current (µA)	25	25

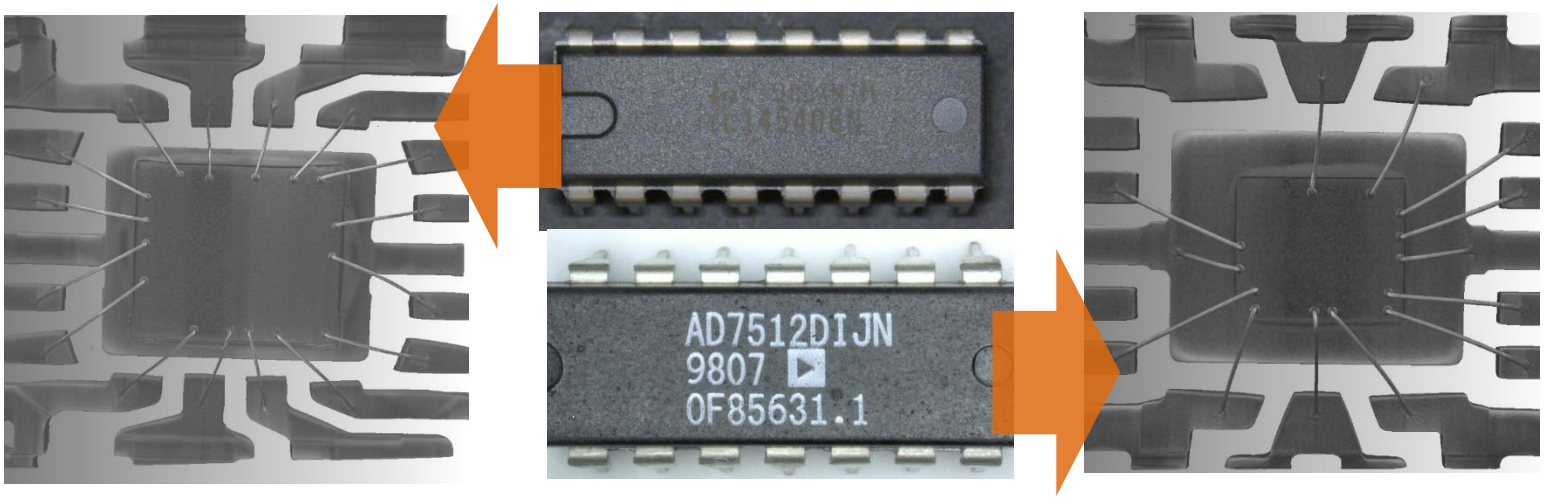
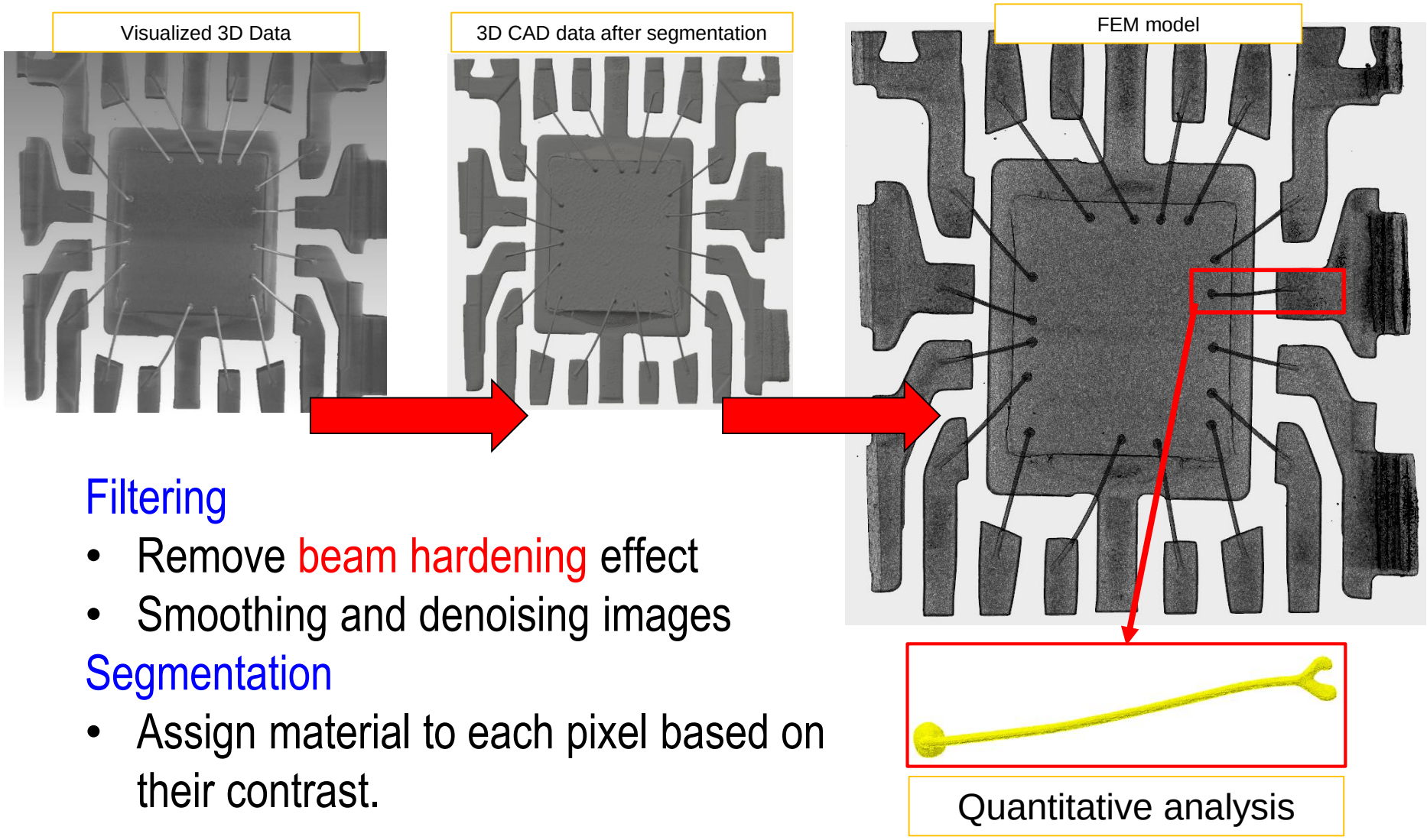


Image Filtering and Segmentation



Filtering

- Remove beam hardening effect
- Smoothing and denoising images

Segmentation

- Assign material to each pixel based on their contrast.

FE Model Information

There are three different types of bond wire failures:

1. Wire break at bond heelcrack or neck break on ball bond or stitch side.
2. Wire break that occurs on any place other than the previous two cases.
3. Bond lift off from pad metallization on ball bond or stitch side. (X-ray resolution is not enough to resolve the details for this item.)

- The first two can be easily detected using the proposed method
- Autodesk Simulation Mechanical 2017 software is used for quantitative analysis

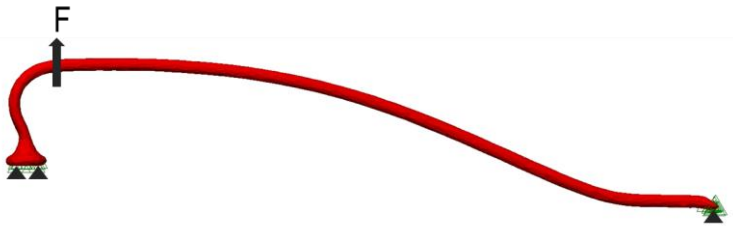
loop-part (l), loop-height (h)

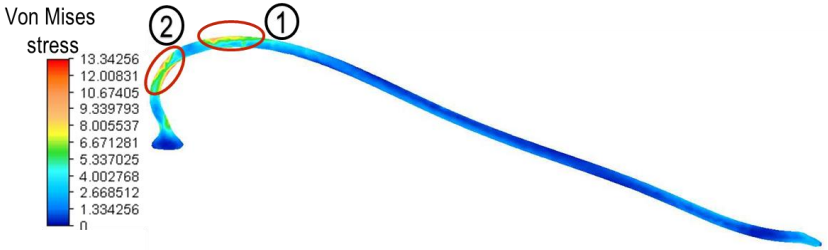
Bond wires meshing information

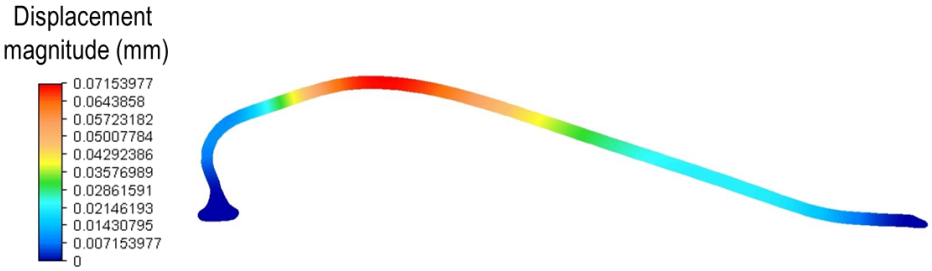
Chip type	TL 145406N		AD7512DIJN	
	Wire 1	Wire 2	Wire 1	Wire 2
Mesh size (μm)	6.1	6.8	16.1	18.09
Total elements	40468	34195	10225	5154
Total nodes	9855	8526	3047	1664
Loop-part (μm)	30	29	72	46
Loop-height (μm)	179	183	254	257
Diameter (μm)	26.4	23.7	31.2	30.3

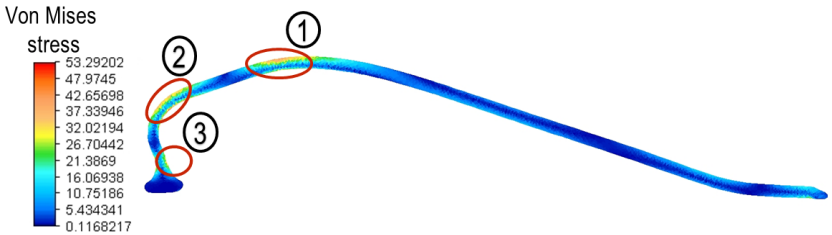
FE Analysis

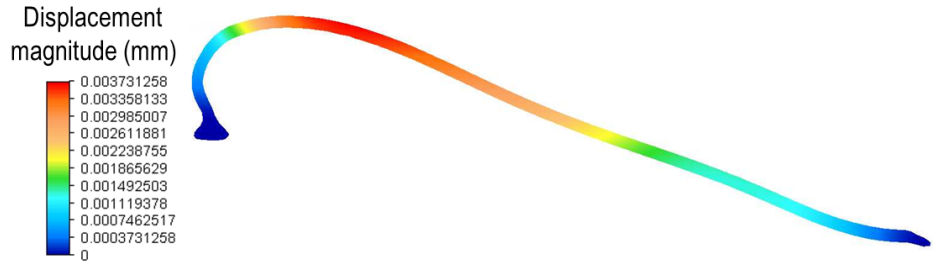
- Initial and boundary conditions are applied to bond wires
- Both ball bond and stitch side are fixed
- 1 cN Load is applied to the bond wire
- Stress and strain in wires are investigated after applying the force







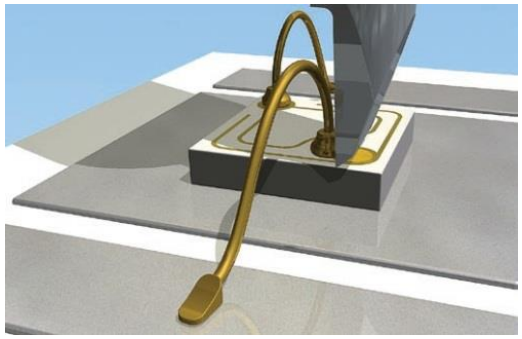




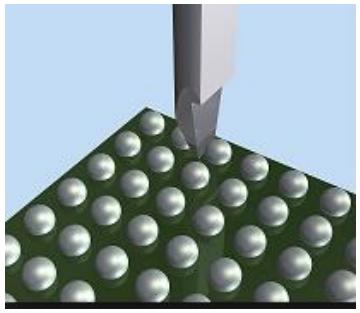
Maximum values for stress and strain are still in an acceptable range

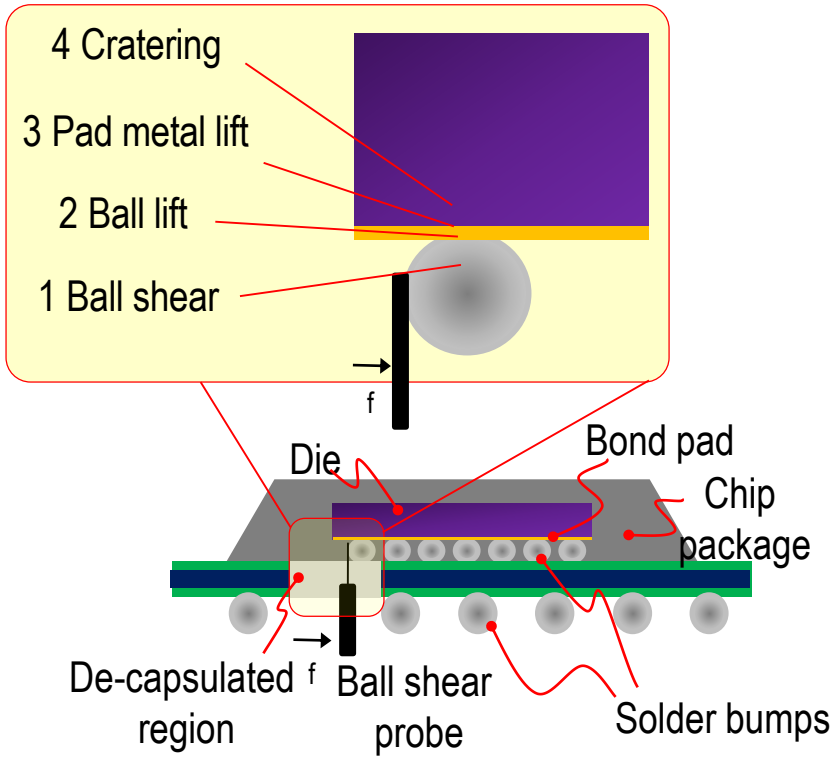
Extension to Ball Shear Testing

Ball bond shear on bond wire



Ball bond shear on ball grid array





Disadvantages

1. Package should be entirely or at least partially removed
2. Each ball bond can be used for only one test
3. Durability and Fatigue Analyses require long testing times
4. The effect of mechanical load is exerted on one bond ball at a time

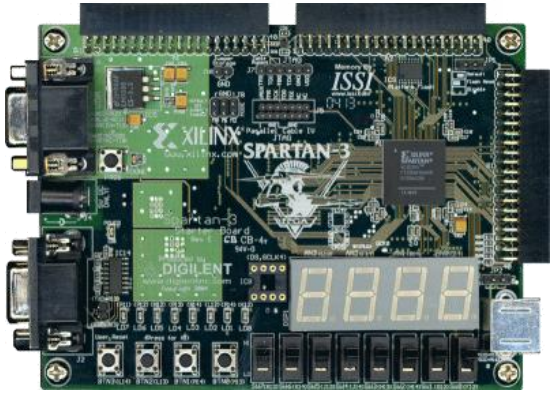
X-ray Tomography Reliability

Experimental Setup

- Selected Integrated Circuits are:

1. Flash Memory
   a) Intel 28F400B5 (400nm Technology)
   b) Macronix MX29F400C (150nm Technology)

2. FPGAs
   a) Xilinx Spartan 3 (90nm Technology)
   b) Xilinx Spartan 6 (45nm Technology)

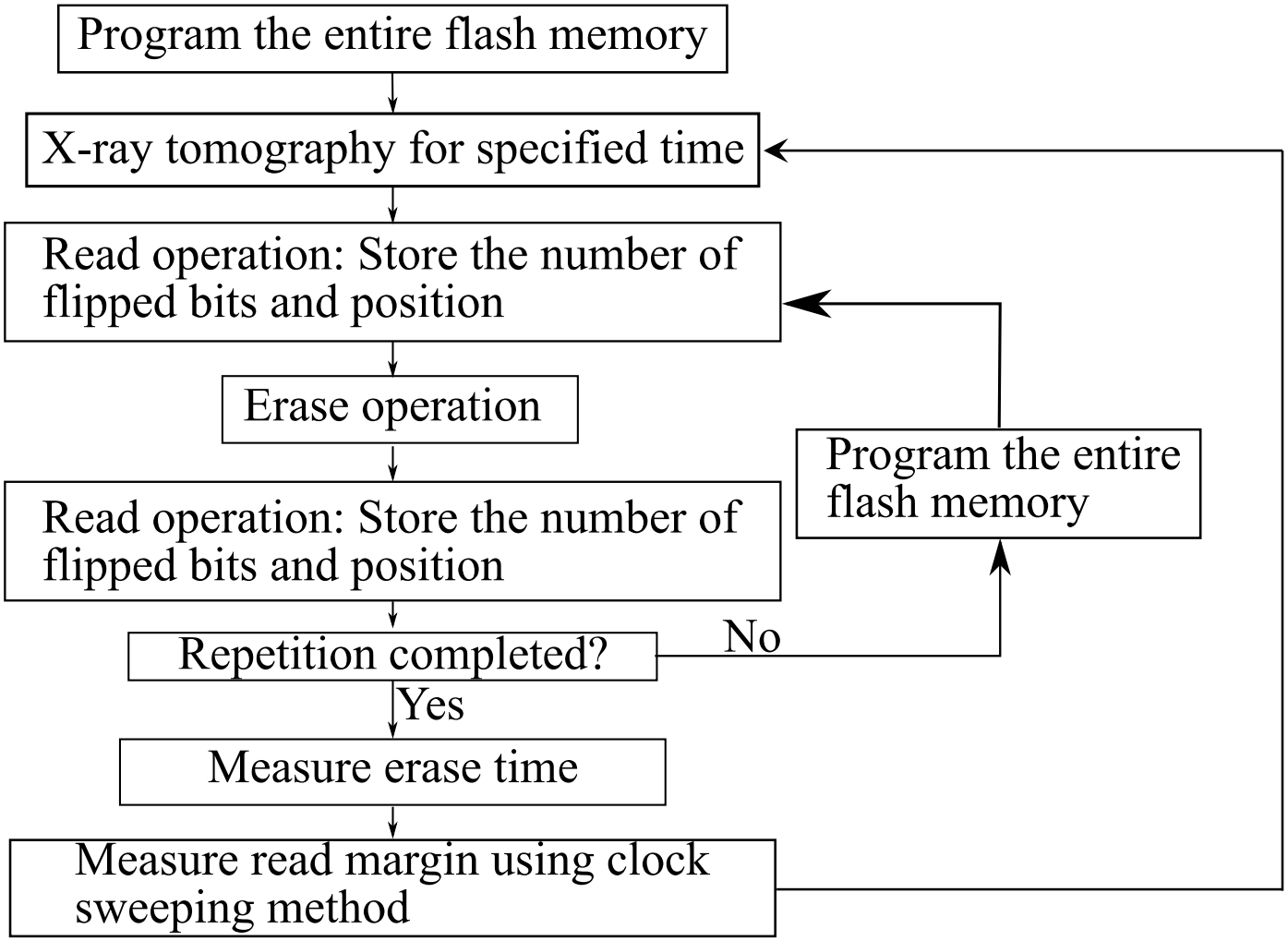


- Total flash memory :

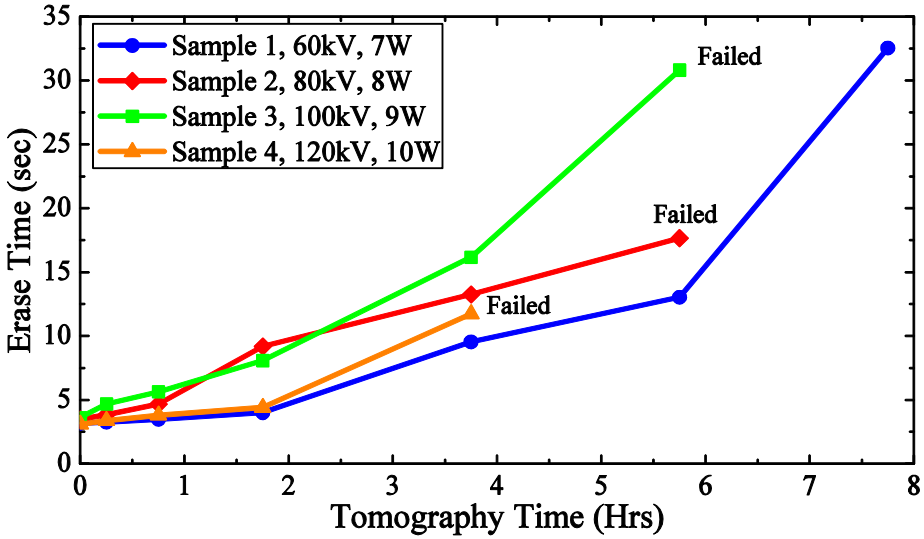
12 (3 sets with 4 ICs in each set)

- Total FPGAs: 4.

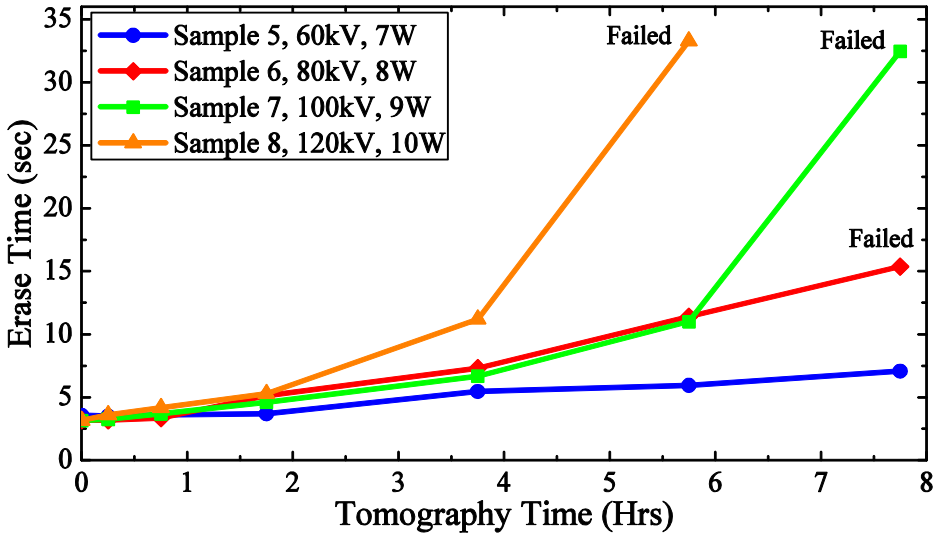
Electrical Tests of Flash Memory



Results of Flash Memory



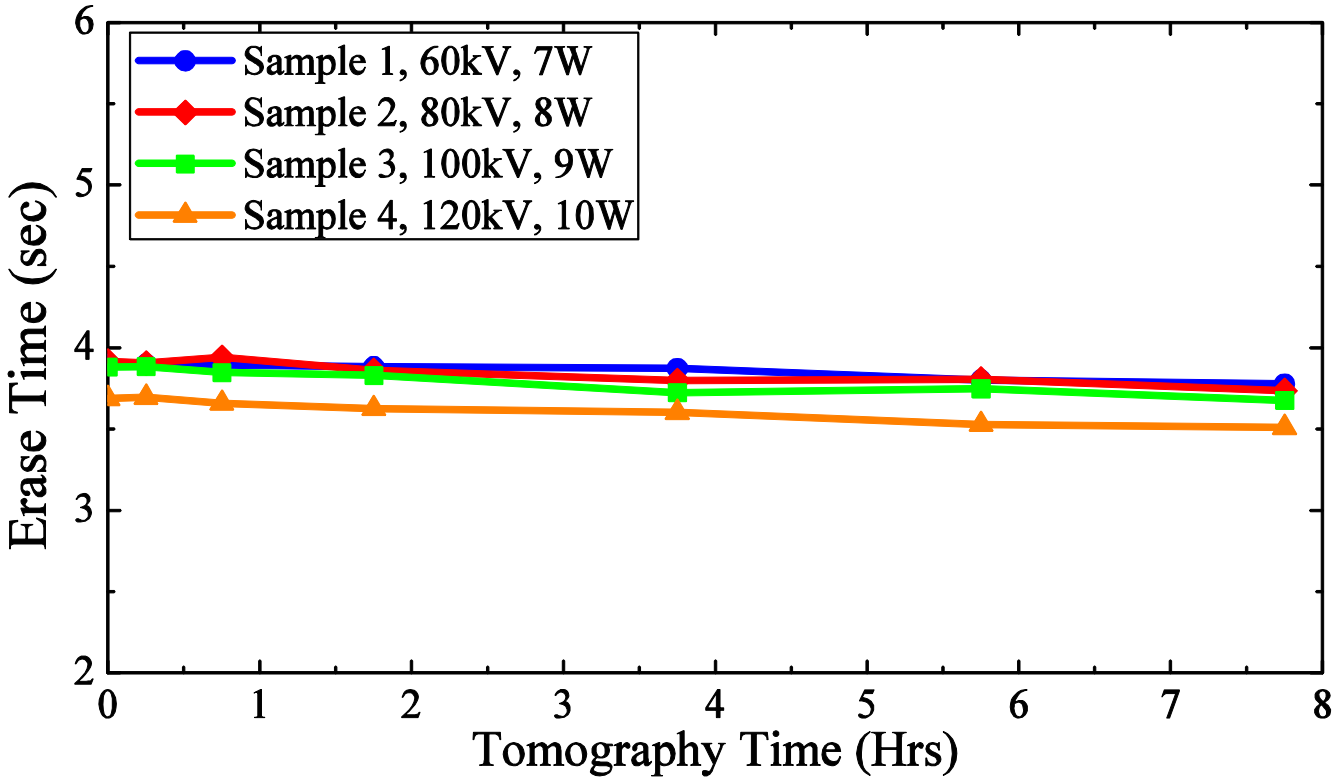
Change in erase time for Set-1 Intel flash memories.



Change in erase time for Set-2 Intel flash memories.

- No bit flip and no change in read margin.
- Read operation is not affected.
- Erase time increased exponentially.
- Failure of erase operation occurred.

Results of Flash Memory

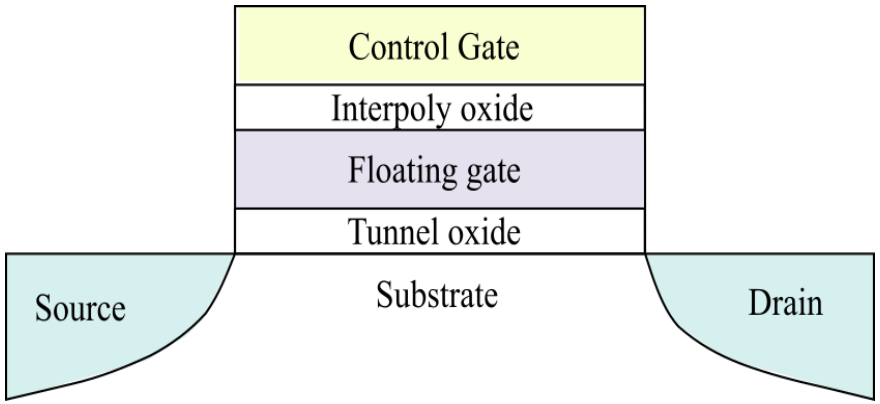


Change in the erase time for Macronix flash memories.

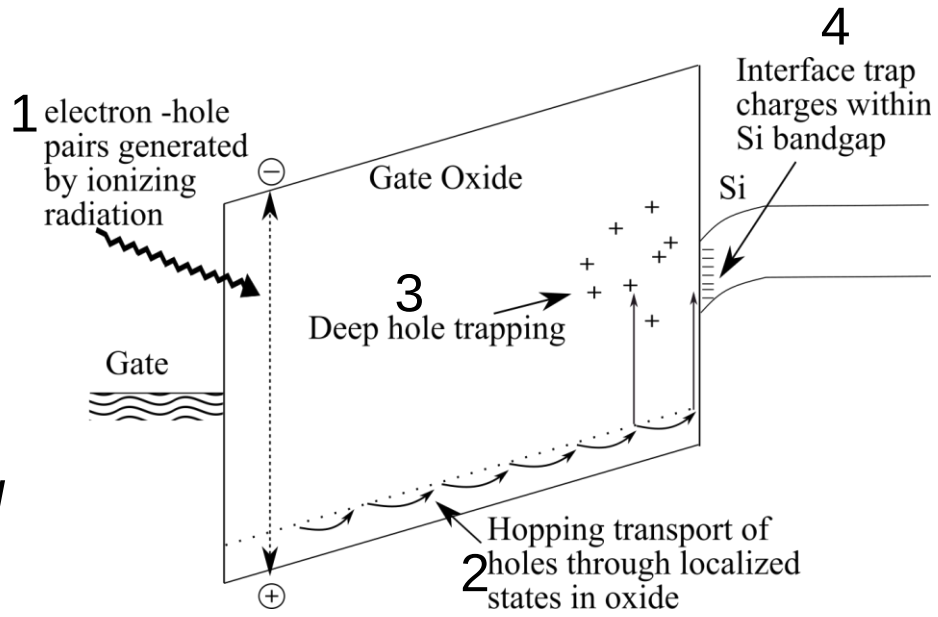
- Negligible change in Erase time.
- No Failure of erase operation.

Discussion of Flash Memory Result

Trapped charges in tunnel oxide of Floating Gate Transistor (FG)



Standard floating gate memory cell

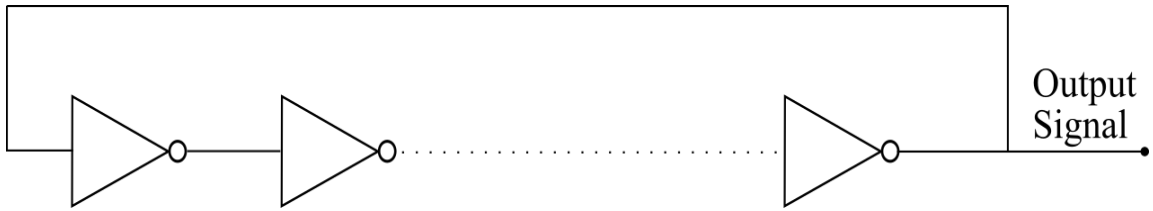


Sources of degradation

Oxide and interface trapped charges.

Electrical Tests of FPGAs

- Tomography was performed at unbiased FPGAs.
- Test focused on the change in the speed of FPGAs.
- Ring Oscillators (ROs) were placed into FPGAs to measure delay of Configurable Logic Blocks (CLB).



RO with odd number of inverters

$$f_o = \frac{1}{2\sum_{i=1}^{n} \tau_{d,i}}$$

$t_{d,i}$ delay of each element

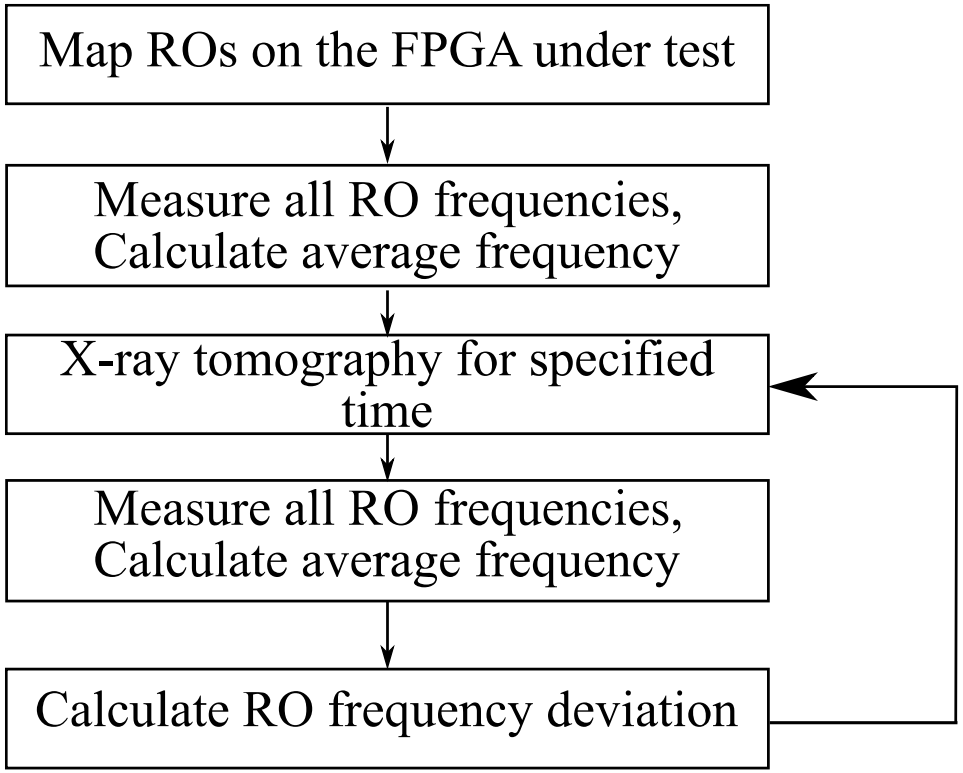
Electrical Tests of FPGAs

Frequency Deviation

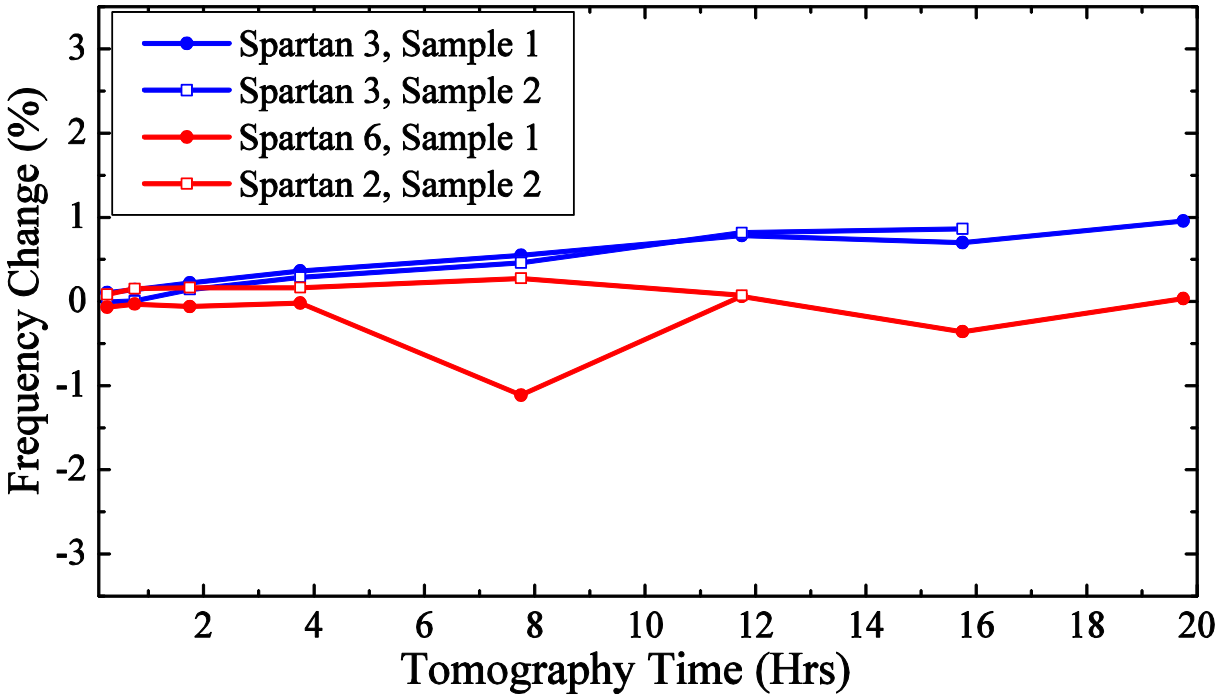
$$\Delta f_{i,t_n} = 100 \times \left(\frac{f_{i,t_n} - f_{i,t_o}}{f_{i,t_o}}\right)$$

f_{i,t_o} initial frequency of *i*th RO

f_{i,t_n} frequency of the *i*th RO after the *n*th tomography cycle.



Results of FPGAs



Percentage change in the frequency in Spartan 3 and Spartan 6 FPGAs

- Average RO frequency increases with time for both Spartan 3 FPGAs.
- Negligible change until first 4 hours of time in Spartan 6.

Reading

- USENIX paper: Printed Circuit Board Deconstruction Techniques
- IEEE TCPMT paper: PCB Reverse Engineering Using Nondestructive X-ray Tomography and Advanced Image Processing
- ISTFA paper: Non-destructive Bond Pull and Ball Shear Failure Analysis Based on Real Structural Properties
- ISTFA paper: Analyzing the impact of X-ray tomography for non-destructive counterfeit detection