Nano-probing and EBIC/EBAC

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Physical Inspection and AttacKs on ElectronicS (PHIKS)

Presented by: Nitin Varshney

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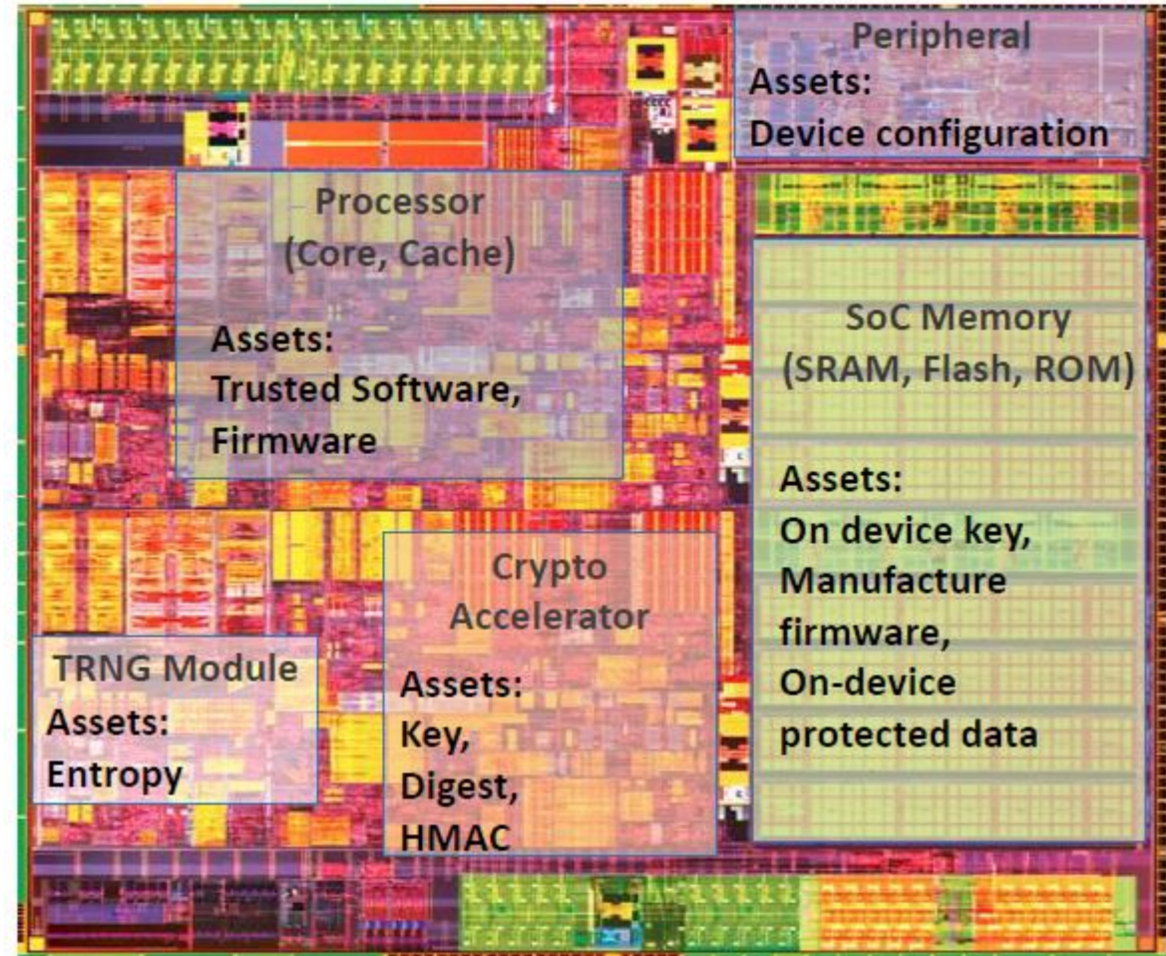
Critical Assets in SoCs

Asset: A resource of value worth protecting from an adversary

Examples:

- On-device keys (developer/OEM)
- Device configuration /defeaturing
- Manufacturer firmware
- Application software
- On-device sensitive data
- Communication credentials
- Random number or entropy



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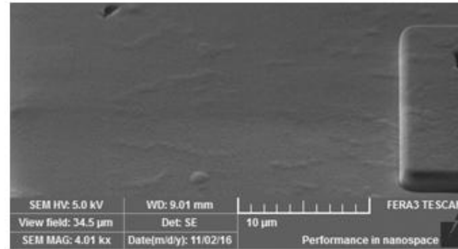
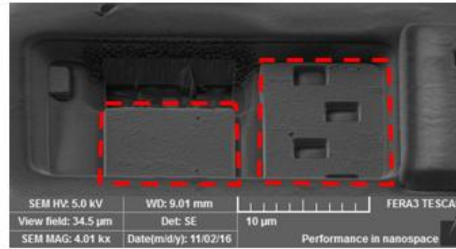
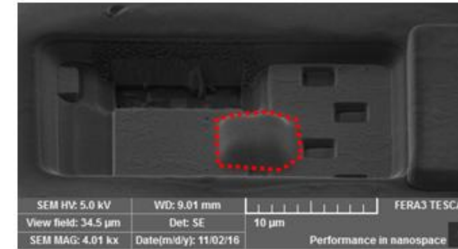
Rise of Invasive attacks



Pre-FIB surface



FIB milling to expose adjacent interconnects



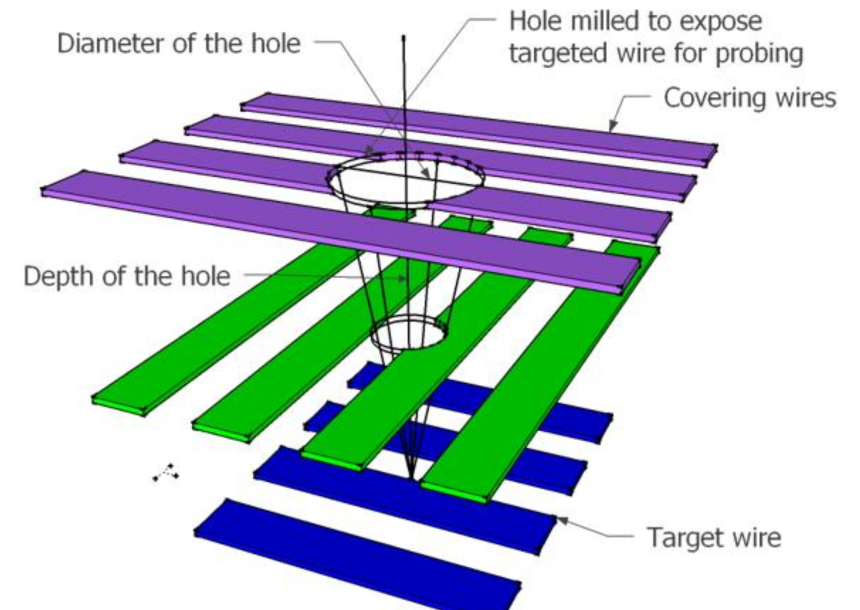
FIB deposition to short adjacent interconnects

Focused Ion Beam (FIB)

- A powerful tool commonly used in the development, manufacturing, and editing of ICs

Micro-probing / editing Attack

- Probing at signal wires to extract security sensitive information
- Front-side attack and back-side attack



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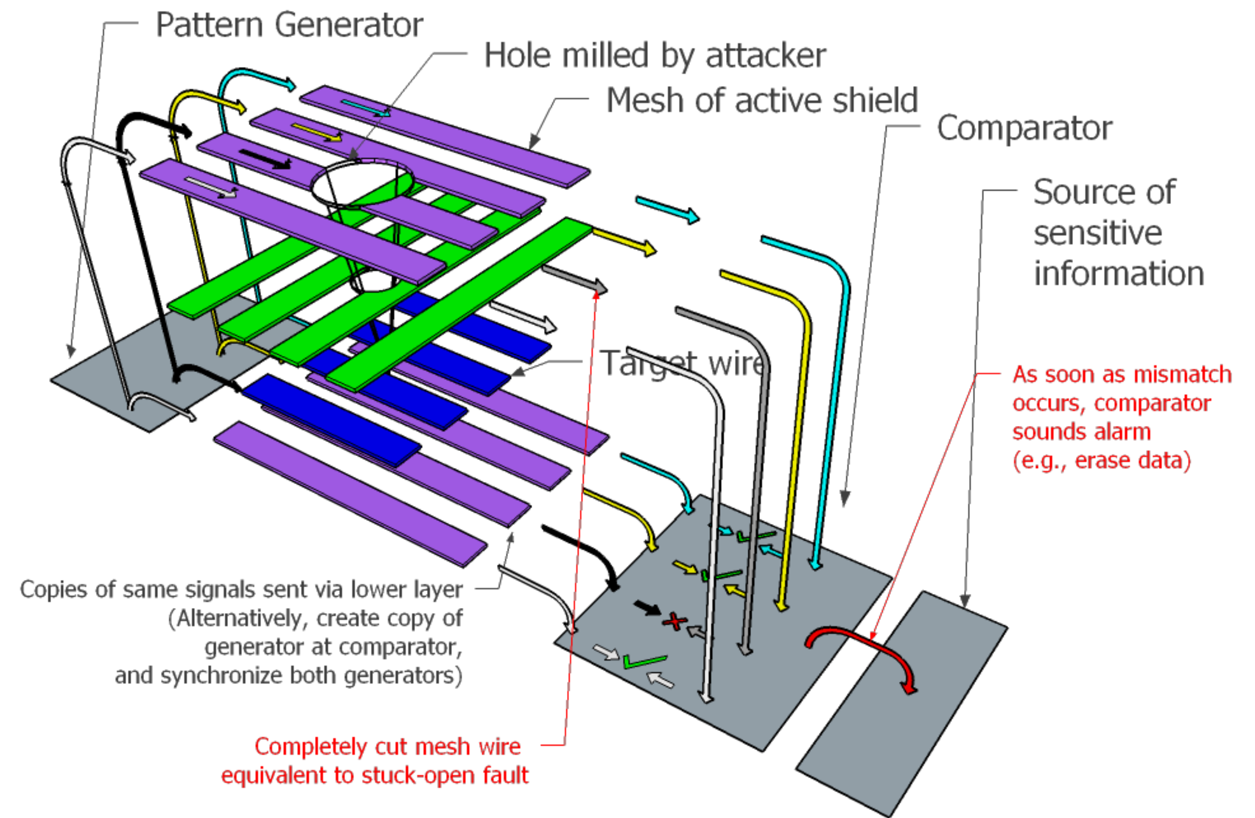
Active Shields

Limitations

- Occupy at least one routing layer, costly.
- Could be easily bypassed by the FIB with high aspect ratio.
- If the shield structure can be reverse engineered, it's vulnerable to reroute attack.
- The shield could be disabled by editing its control circuit.
- Only protects against front-side attacks.



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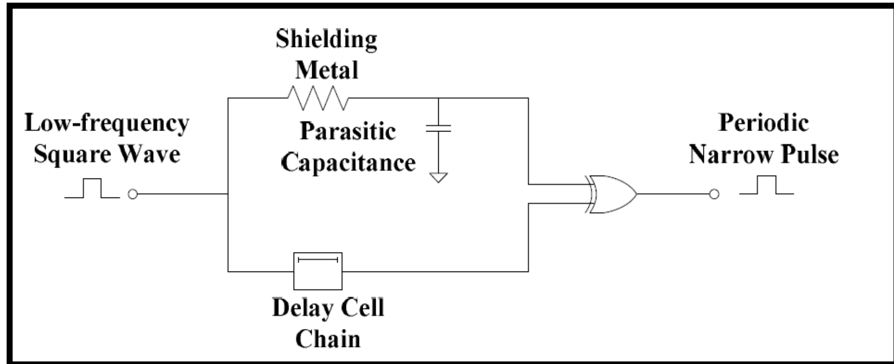
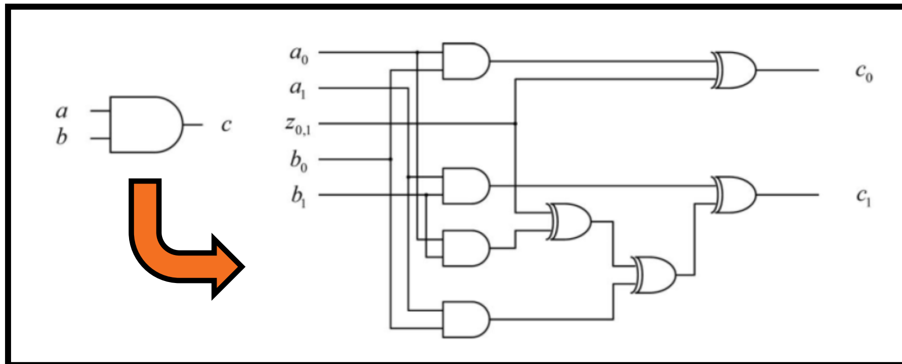
Analog Shields and t-Private Circuits



Limitations

- Unreliable due to process variation especially with feature scaling



Limitations

- Large area overhead ($O(t^2)$)

Summary

- Existing countermeasures are limited and/or expensive
- No notion of what is most in need of protection
- No approach can be easily incorporated into conventional design flow

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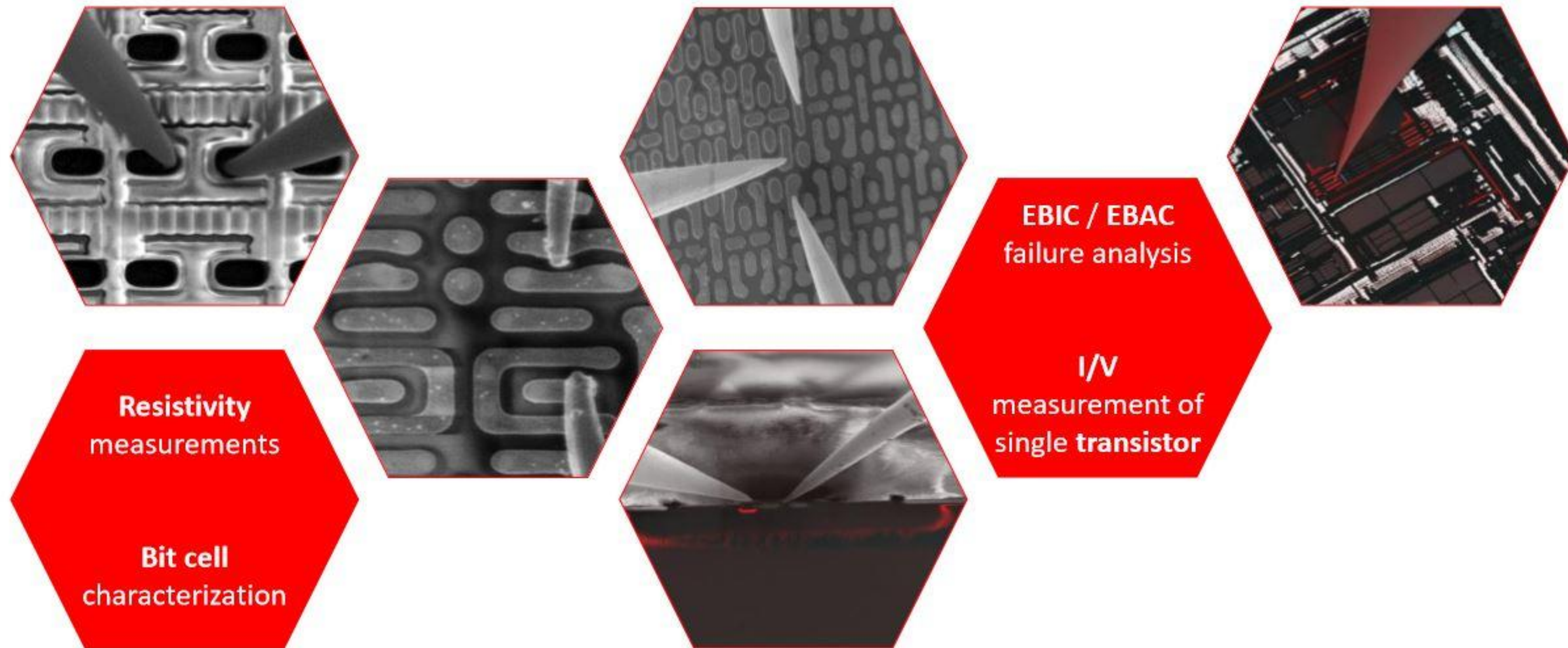
Applications of Electrical Probing in Semiconductors

1. Nanoprobing and Failure Analysis



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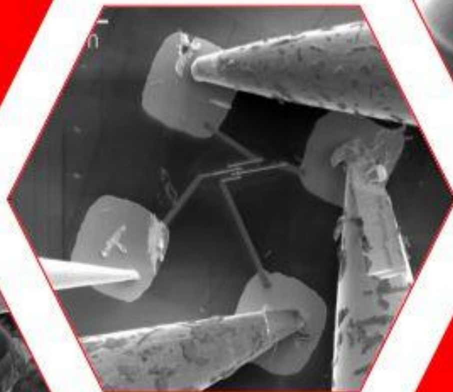
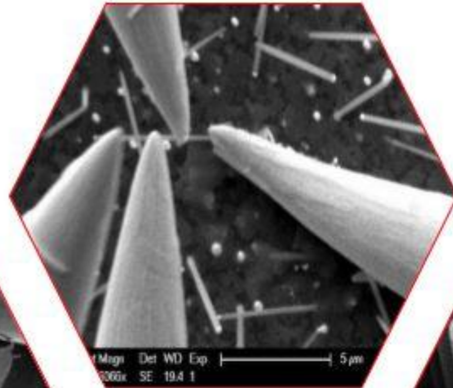
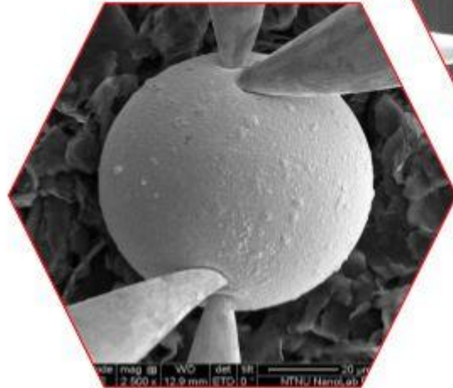
2. Electrical Characterization

4 point probing measurements

Thin film/coating characterization

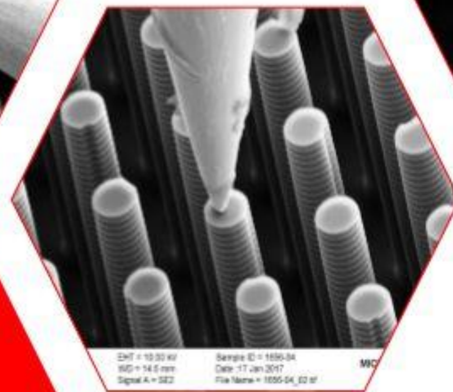


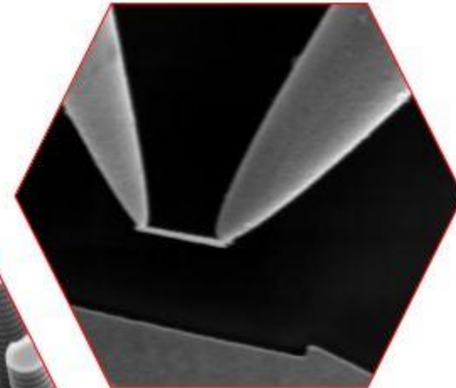




Fragile sample testing

Single structure isolation





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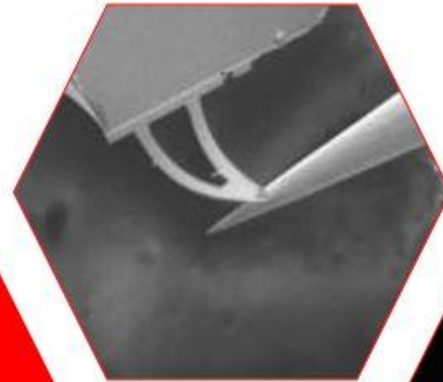
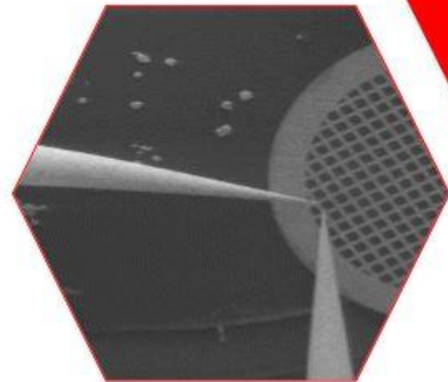
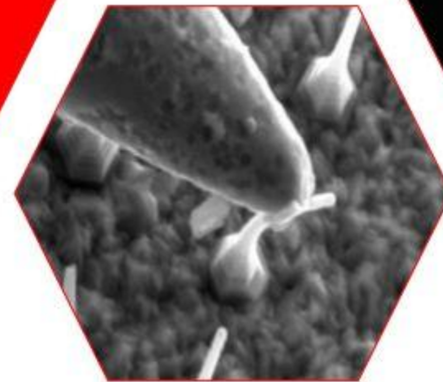
3. Sample Handling and Positioning

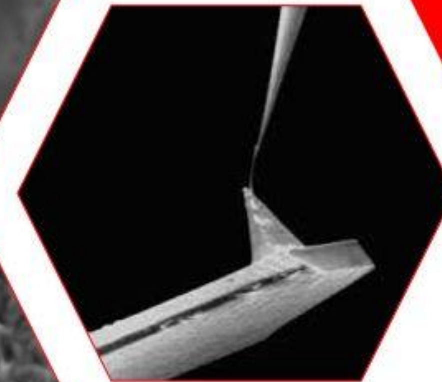
TEM sample preparation

Micro-/Nano manipulation









Nanostructures positioning and assembly

Mechanical testing

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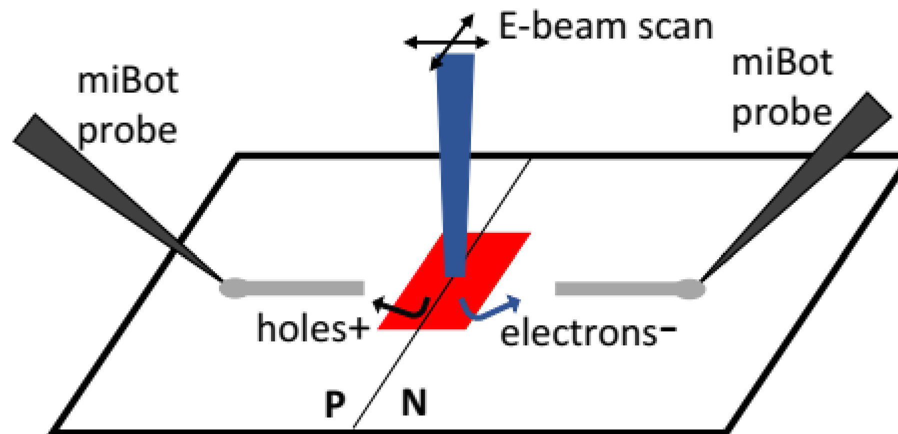
Electron Beam Induced Current

EBIC is a method used for the imaging and characterization of p-n junctions, the recombination strength of defects, and the diffusion length and surface recombination velocity of minority charge carriers in semiconducting materials and devices.

It is most effective when employed alongside EDS or EBSD as part of a wider workflow, for example, nanofabrication in the FIB, or sample preparation for the TEM or atom probe.



Electron Beam Induced Current

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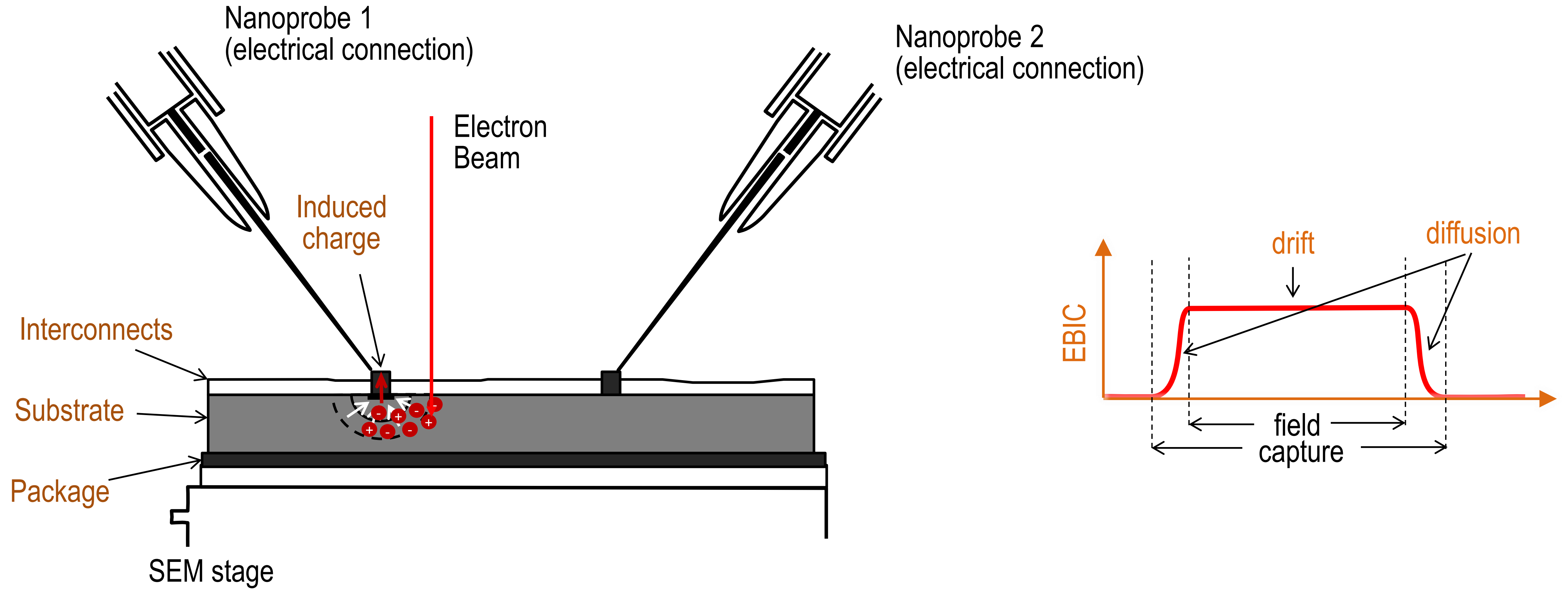
How it Works?



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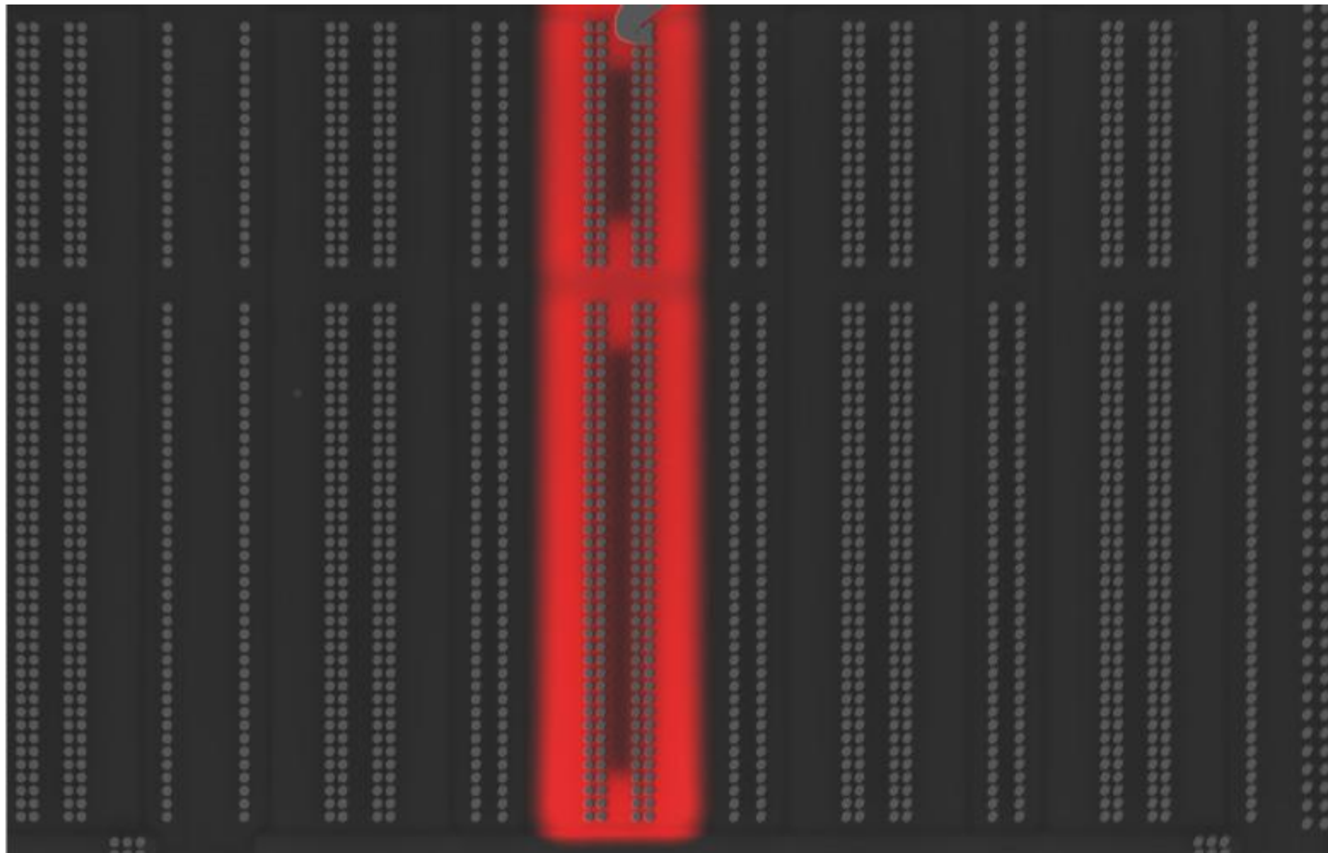
Applications in Hardware Security

Map electric fields with the highest spatial resolution



- Visualise internal electric fields from PN junctions or Schottky contacts.
- Validate doping profiles and areas with design, or reverse engineer devices.
- Identify defects with electrical activity and correlate with structure (SE, In-Lens) and composition (EDS, EBSD).

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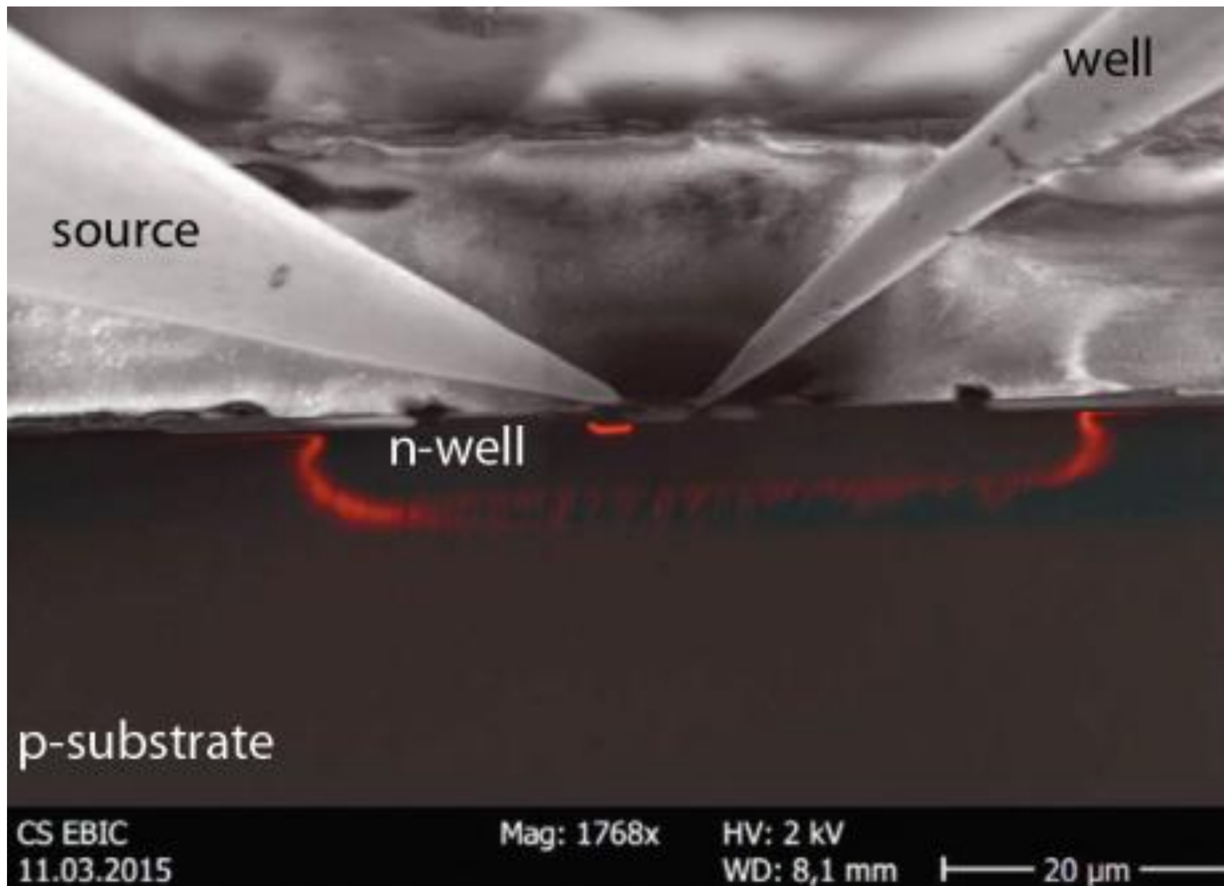
Applications in Hardware Security

Access third dimension with depth profiling.



- Manipulate depth of EBIC signal by changing kV in SEM.
- Investigate EBIC images of cross-sections in FIB-SEM.
- Export EBIC depth series for 3D reconstruction.

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Applications in Failure Analysis

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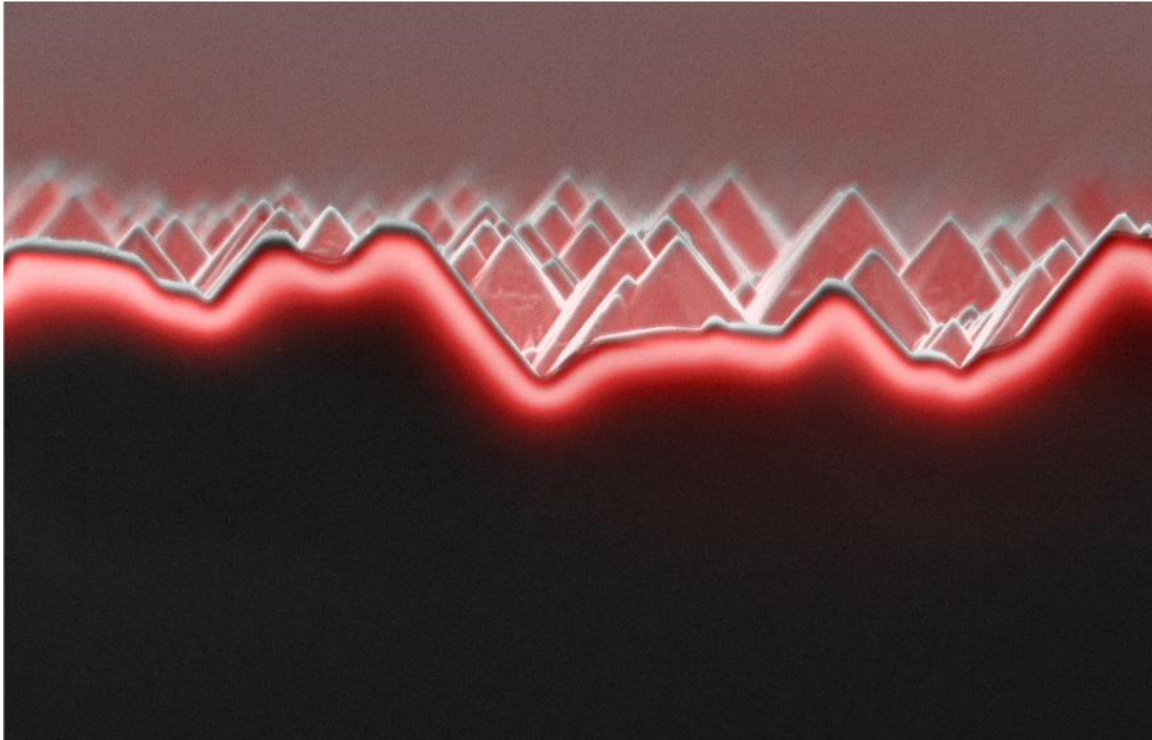
Map complex electric fields on 3D structures.



- Characterise relationship between surface topography and electrical activity.
- Determine internal quantum efficiency from measured induced- and beam-currents.
- Distinguish between active and passive defects – at operating conditions.

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Applications in Failure Analysis

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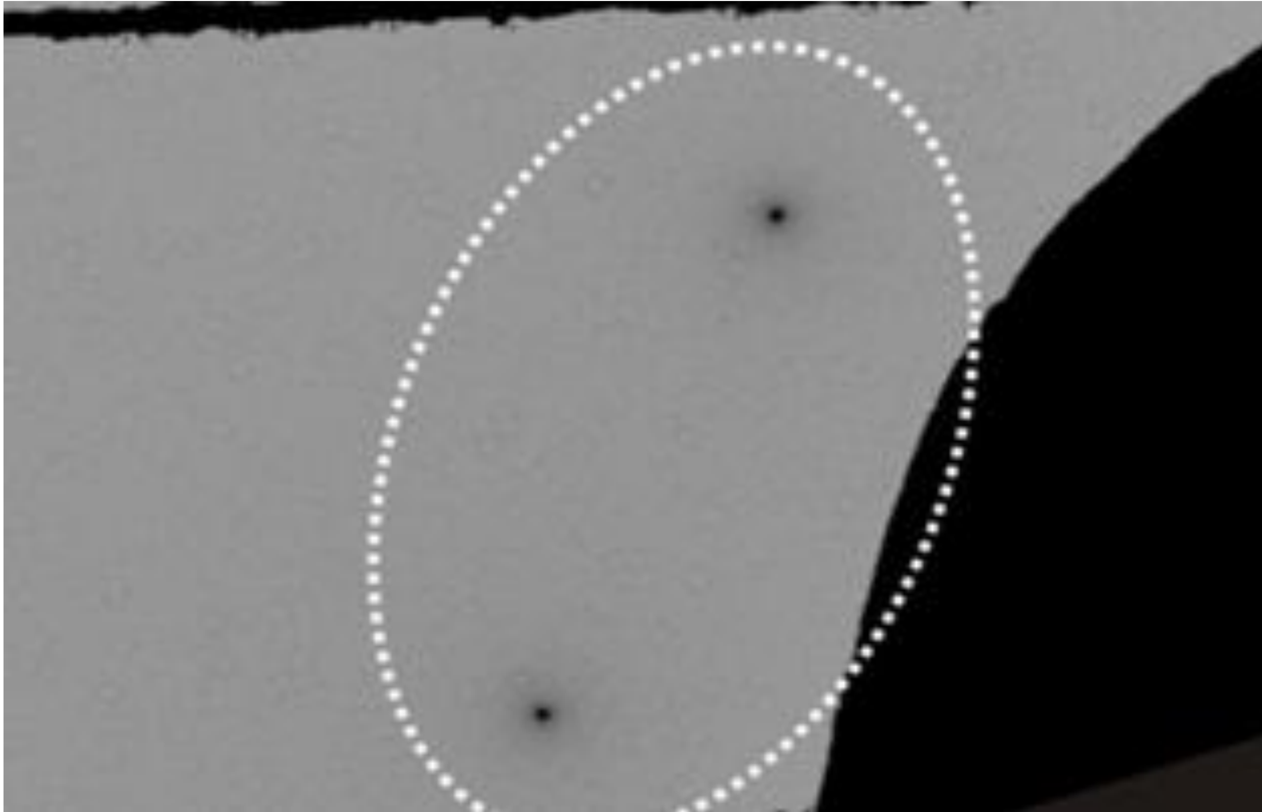
Enable localisation for TEM or atom probe microscopy.



- Localise defects with sufficient resolution for TEM sample prep.
- Avoid alignment errors by directly imaging defects with EBIC in FIB SEM.
- Use live EBIC imaging to stop milling during sample preparation.

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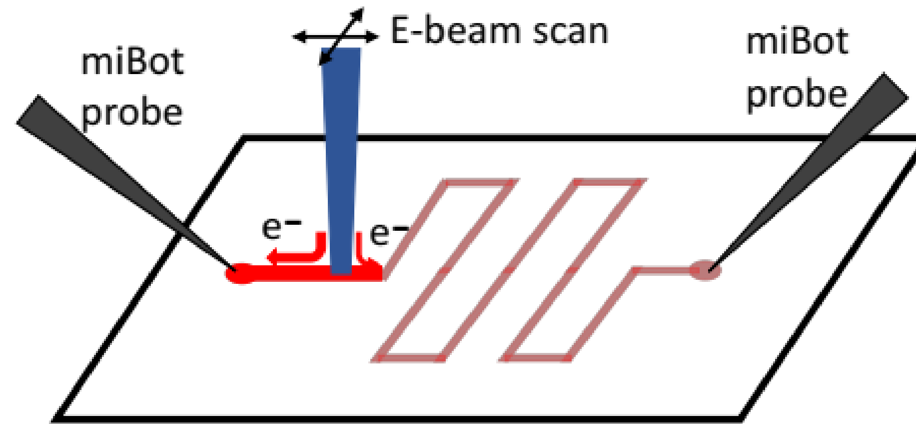
Electron Beam Absorbed Current

EBAC is a method employed for the identification and physical failure analysis of metal defects (opens and shorts), high resistivity areas and layer non-uniformities in CMOS devices. It is primarily used in combination with electrical nanoprobing.

The electron beam of the SEM scans the DUT and injects charges absorbed by metal lines under the surface. A current is then induced and measured by a probe placed with a miBot nanomanipulator at contact level.



Electron Beam Absorbed Current

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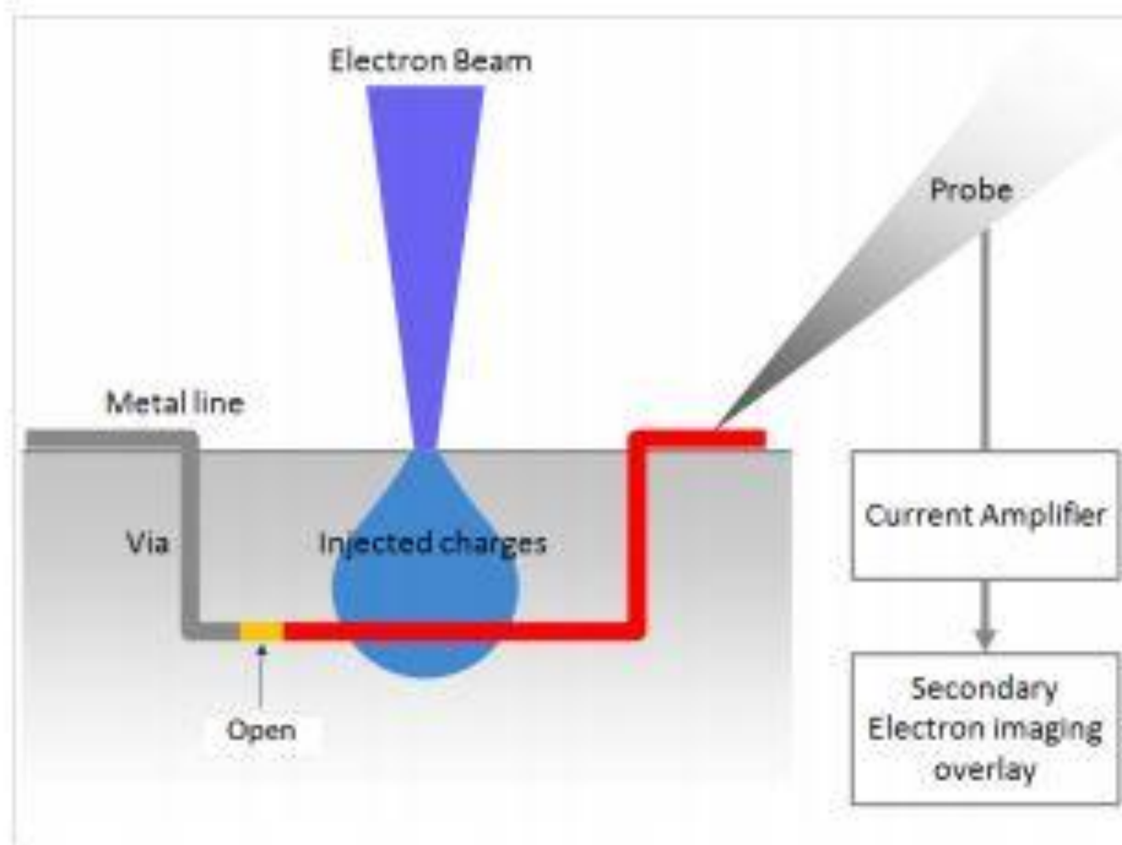
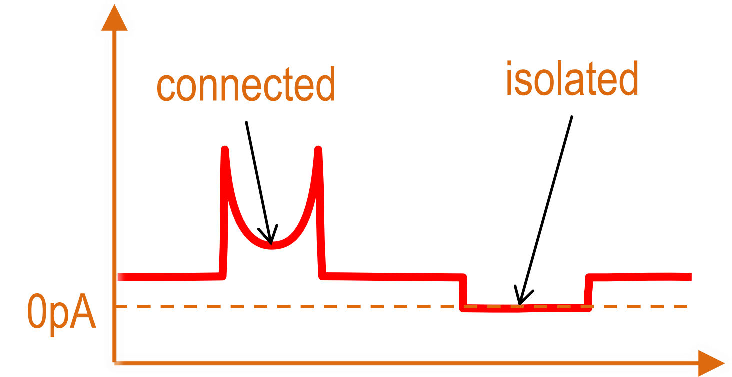
How it Works?





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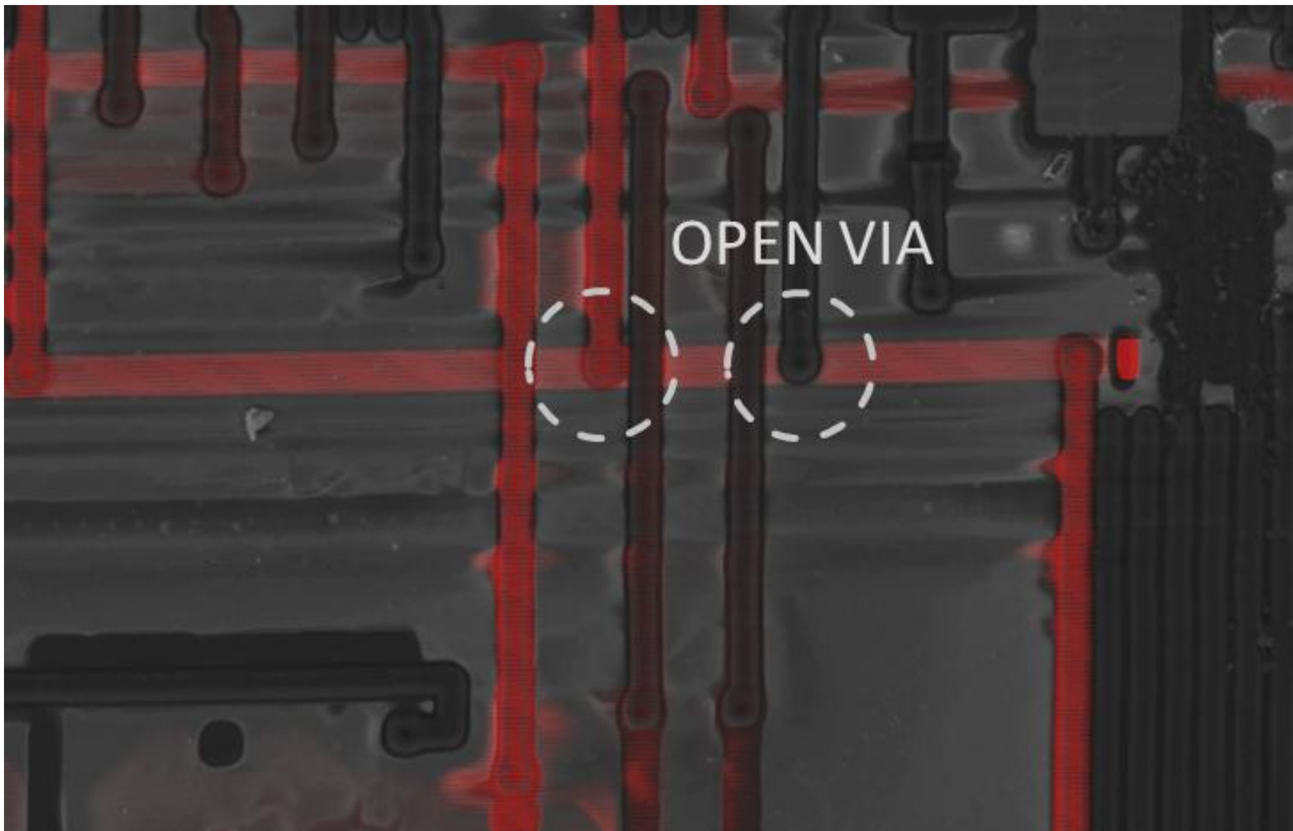
Applications in Hardware Security

Find exact location of any open, resistive or shorting defect.



- Localize cuts caused by cracking, corrosion, electro-migration or particles.
- Identify resistive opens caused by interface contamination at vias.

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Applications in Hardware Security

Characterize interconnects with the highest resolution.

- Reveal electrical integrity of nets with sub-micron resolution.
- Diagnose contamination, metal patterning defects, resistive interconnectors.
- Directly isolate defects to exact layer and die location.

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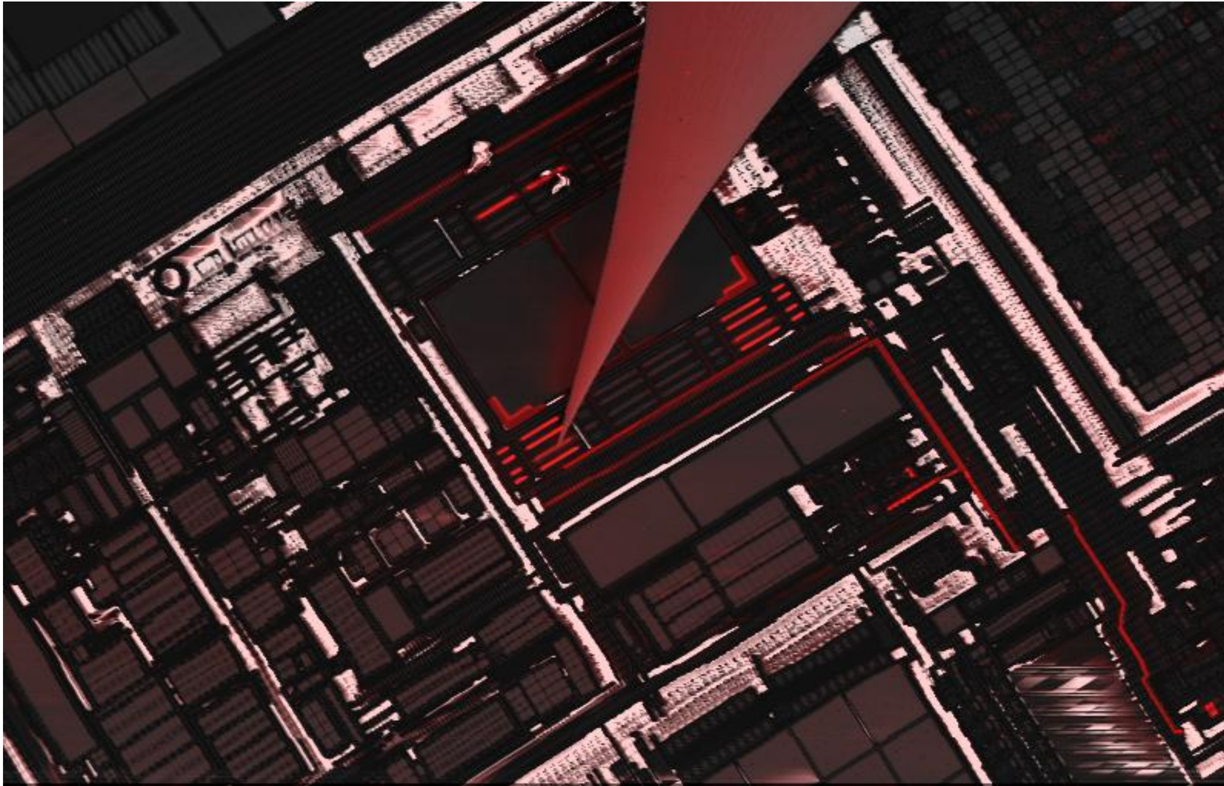
Applications in Hardware Security

Access failures invisible in voltage contrast



- Find low resistances that allow charge tunnelling through interconnects.
- Investigate structures in contact with the silicon substrate.
- Characterize large metal structures

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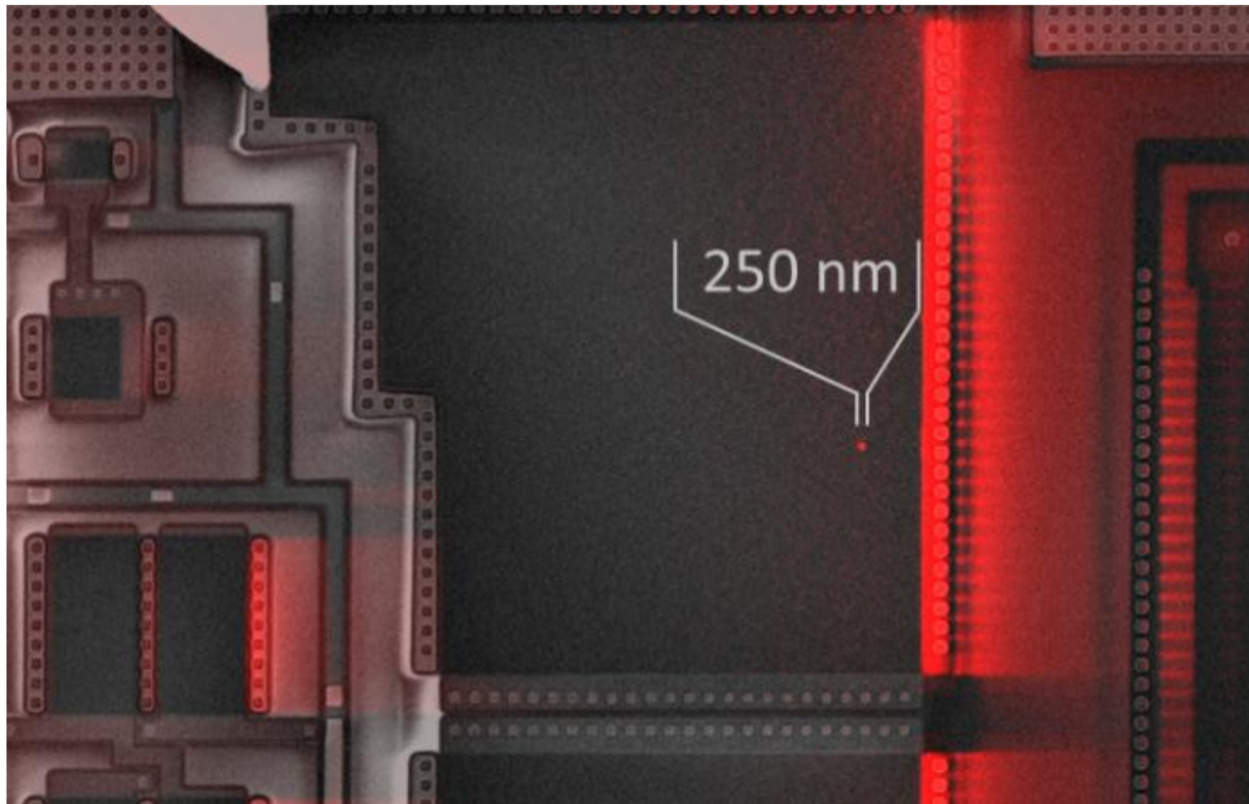
Applications in Failure Analysis

Localize defects in thin dielectric layers.



- Visualize weaknesses in GOX or COX before breakdown.
- Pinpoint oxide shorts caused by ESD or EOS with sub-micron resolution.
- Preserve the original defect with nW power dissipation during analysis.

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Needs in the Semiconductor

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Technologies are shrinking

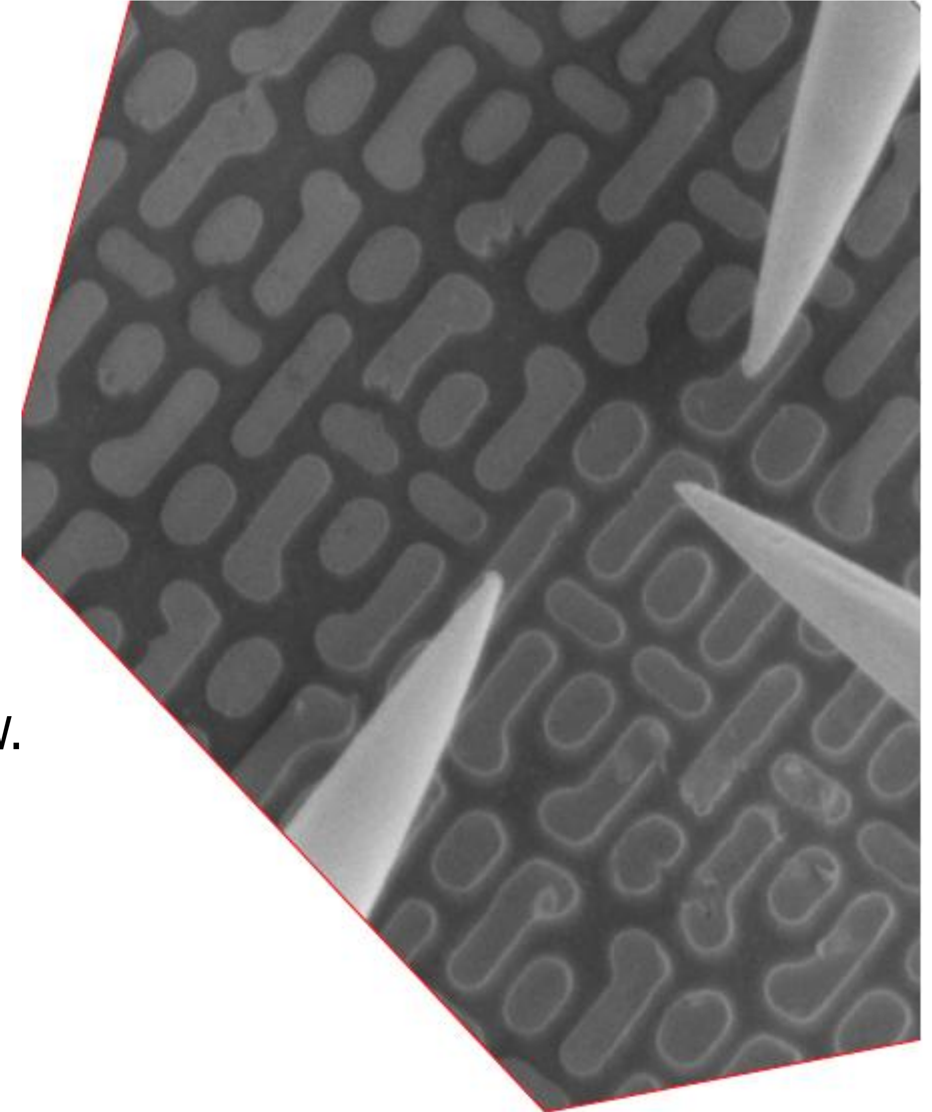
- Nanometer resolution for a precise positioning
- High mechanical stability for steady electrical contacts
- Adapted probes materials and tip radius.

Architectures are becoming complex

- Versatile configuration for a quick adaptation
- Software assistance to guide the operator within the workflow.

Data collection time is limited

- Fast system installation
- Reporting capabilities



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Core technology: a mobile piezo robot

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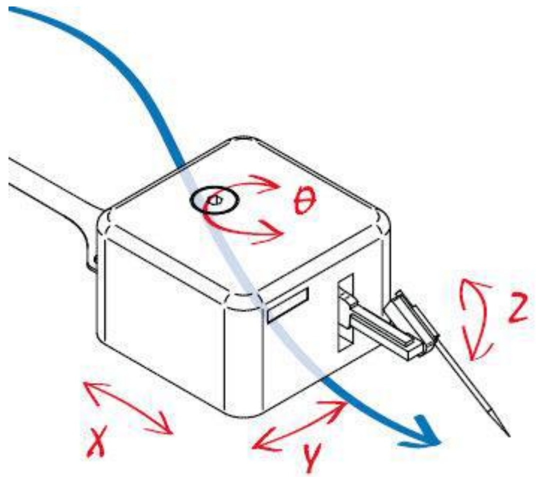
Axis of movement



- Micro to nanometer positioning resolutions
- Centimeter range displacements
- High mechanical stability and near-zero drift
- Freely moving on their stage. Maintained on it with a magnet
- XYZ and rotation movements
- High vacuum compatible
- Can be adapted to different sample size and applications

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Nanoprobing Platform

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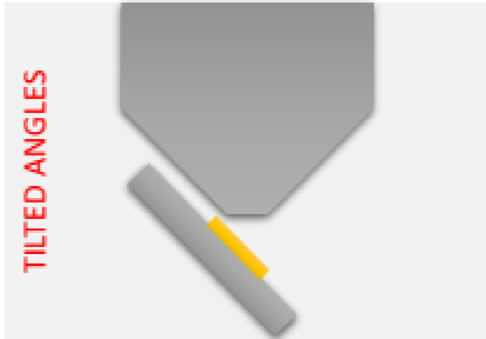

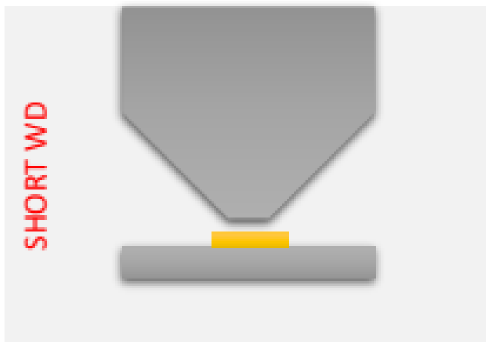

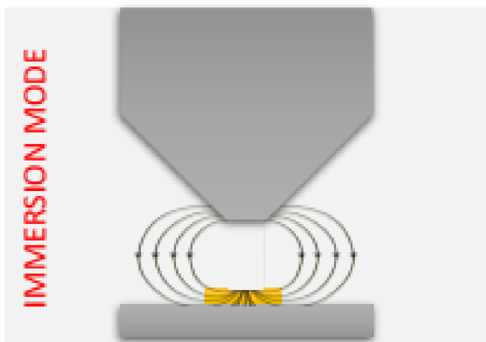

Independent & shielded cabling for excellent signal-to-noise ratio and low-current measurements.

From 1 to 8 independent nanoprobers

Integrated biasing of the sample

Wide range of industry standard probes materials and tip radius

Large and multiple samples with adjustable height for the work at short working distances and low acceleration voltage

Compact and light platforms, compatible with load-lock systems

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Basic Operation Voltage Range

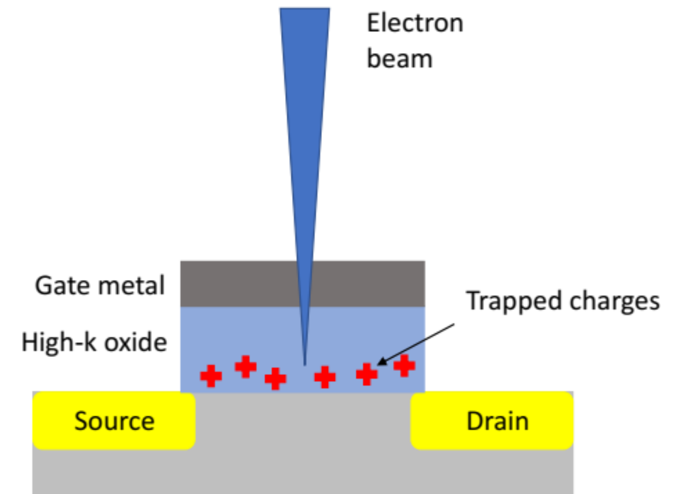
Oxide material sensitive to electron beam:

- Generation of oxide trapped holes.
- Trap generation at the interface.

Results in:

- Shift of the Threshold voltage.
- Increase of leakage current.

Therefore, it is required to image at low KV to avoid changing transistor characteristics. (typically 500V to 1kV depending on technology).



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Challenges

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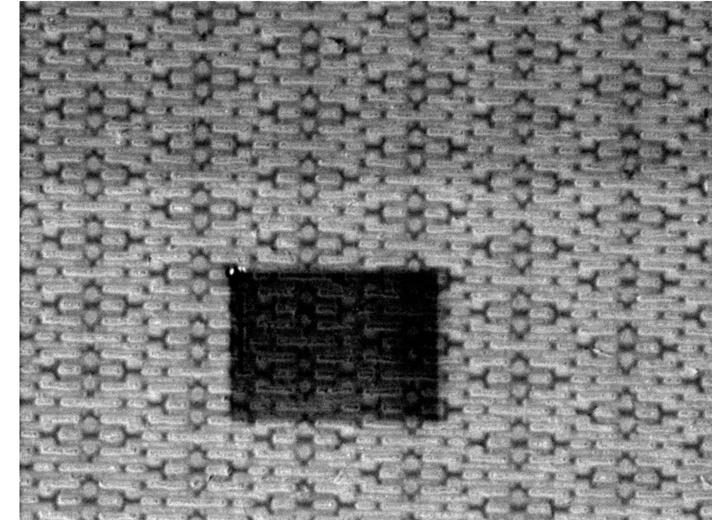

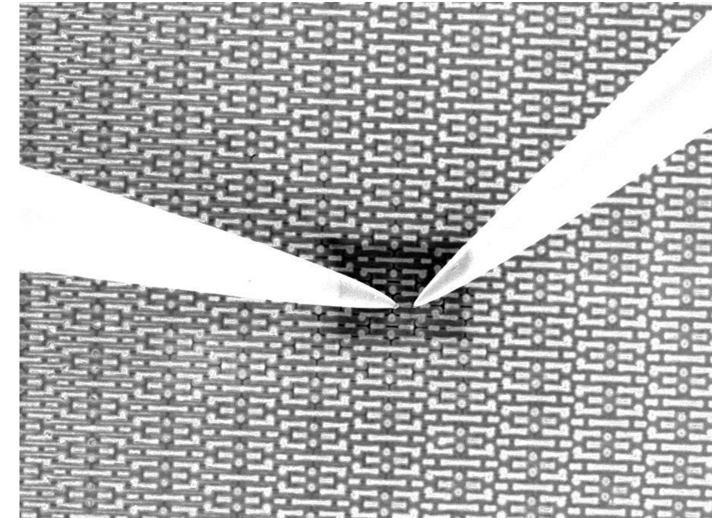

Hydrocarbon contamination

- Inside the chamber
- From outside, when installing new probes, sample, etc.

Contamination has consequences on:

- Imaging quality
- Electrical contact

Suggestions:

- Store the system in a safe environment.
- Use a plasma cleaner to remove hydrocarbon contamination.

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Control Center and Probes Approach

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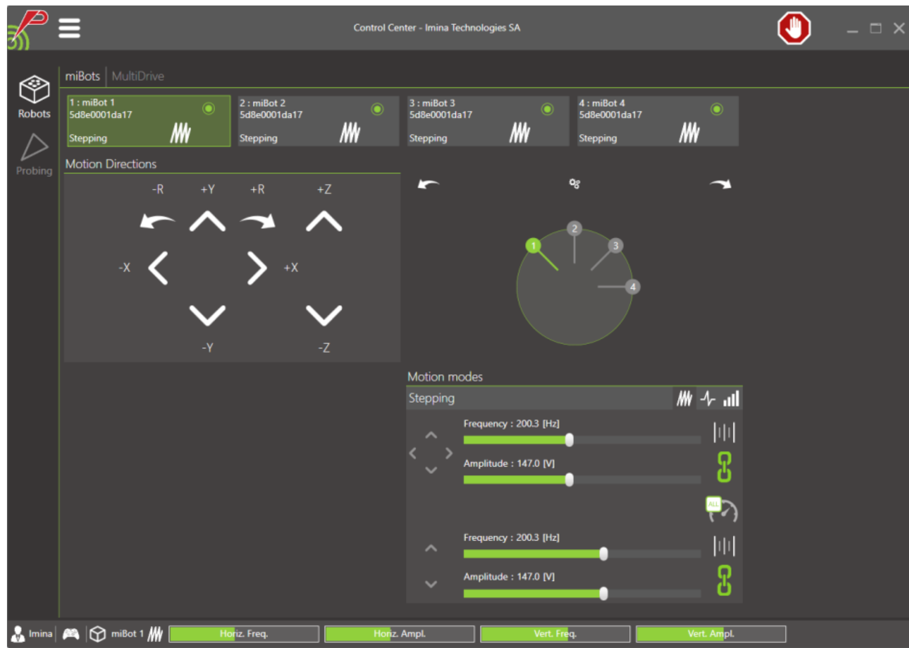

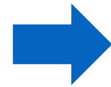

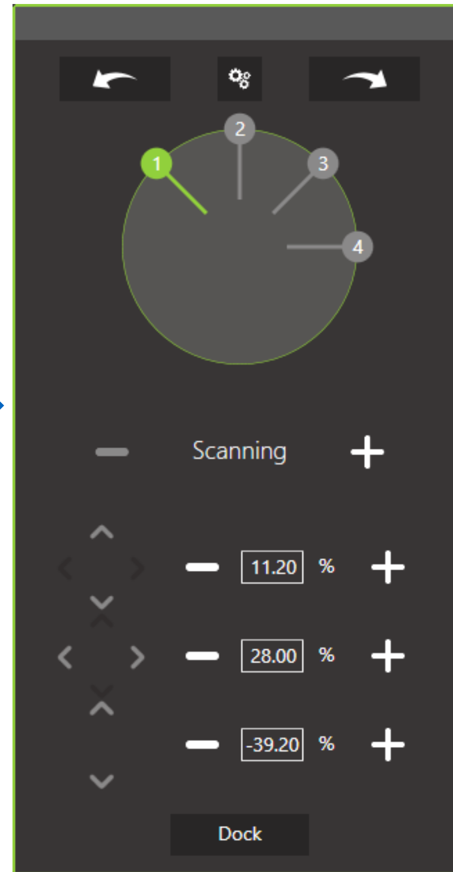

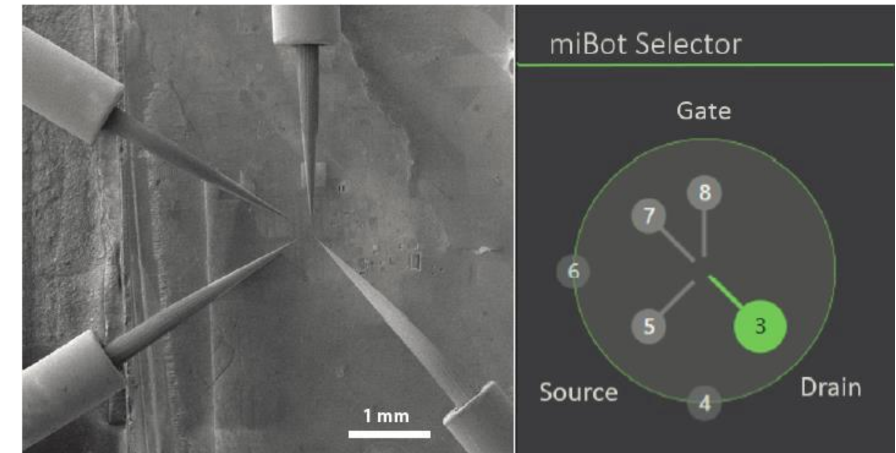

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Steps involved in electrical probing

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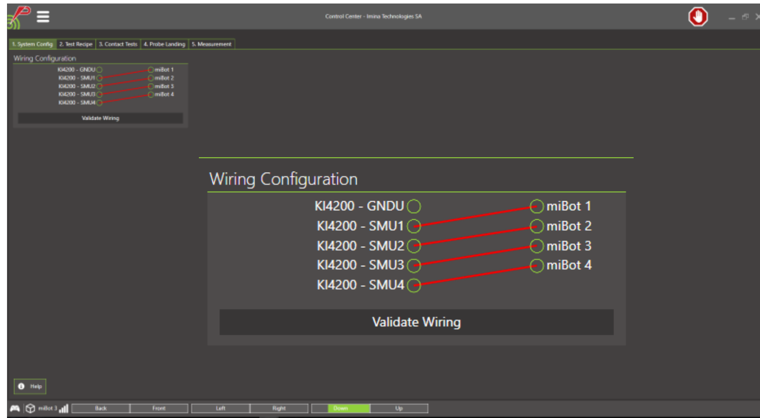
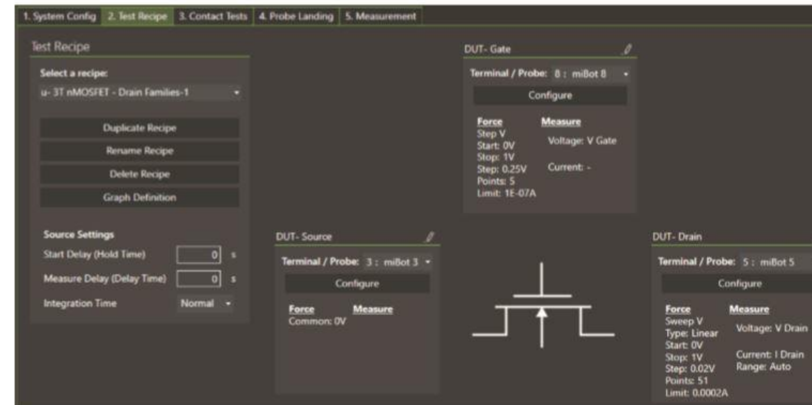
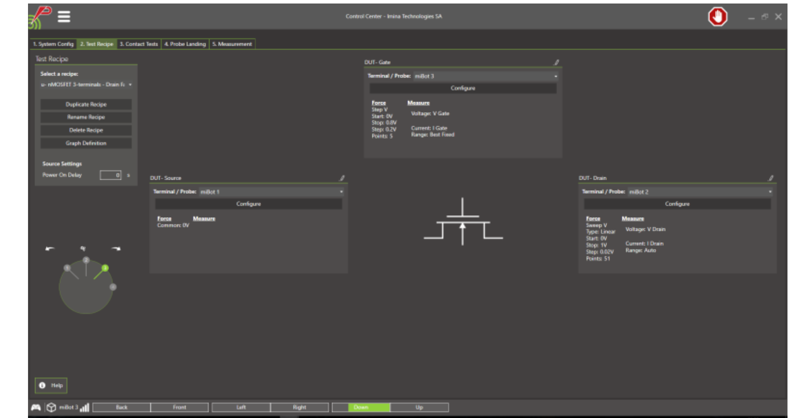


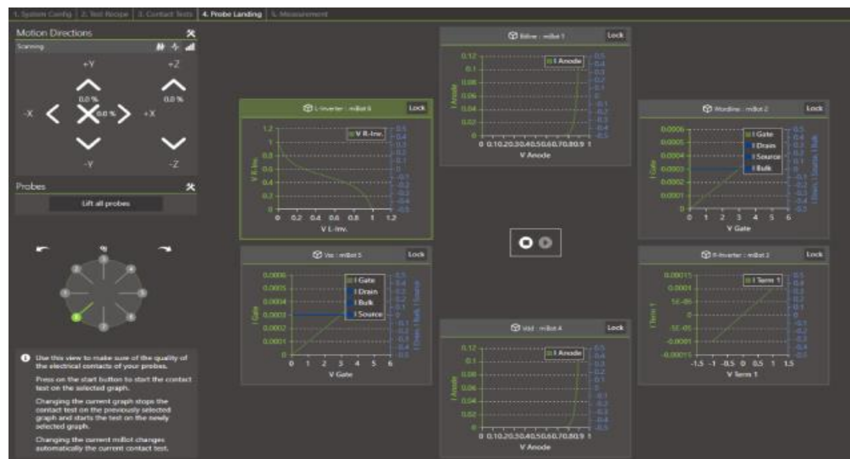
1: System configuration



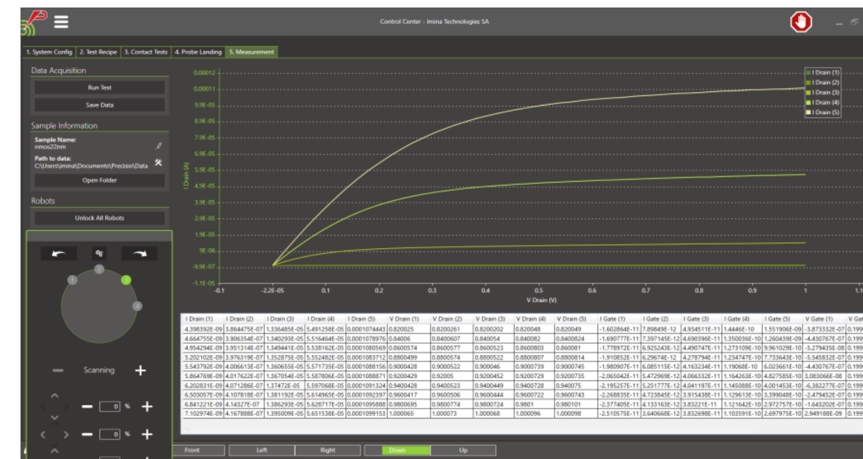
2: Test Recipe



3: Probe Landing



4: Live Contact Testing



5: Measurement & Report

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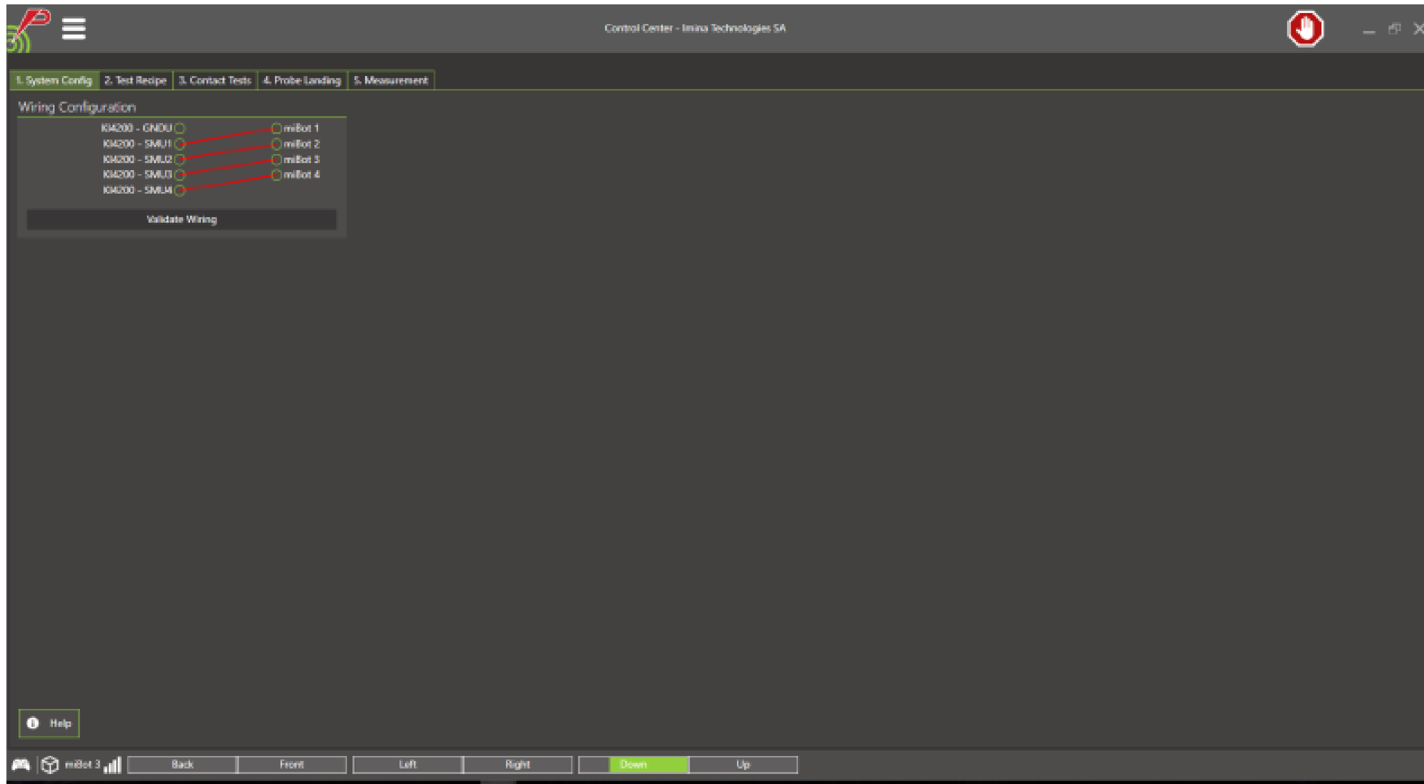
Steps involved in electrical probing



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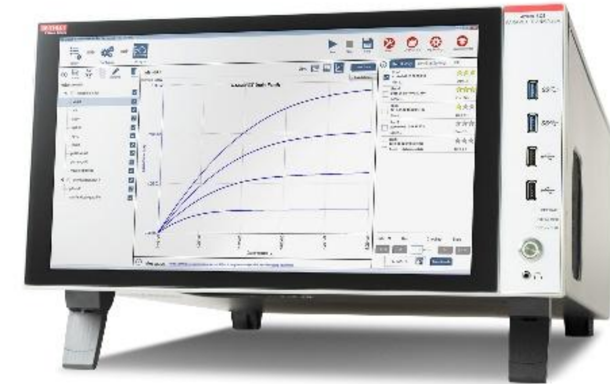
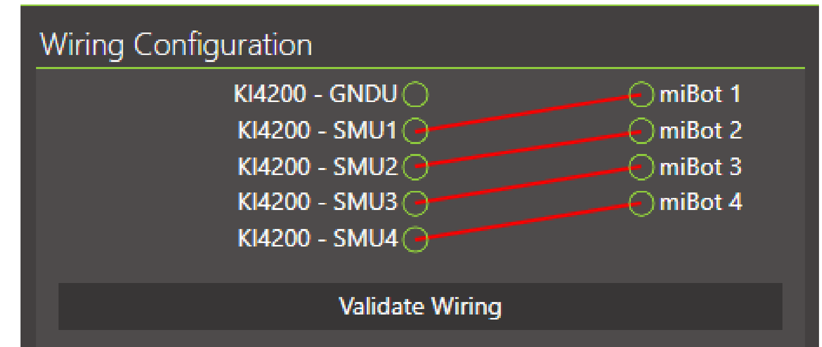


Keithley 4200SA Parameter Analyzer



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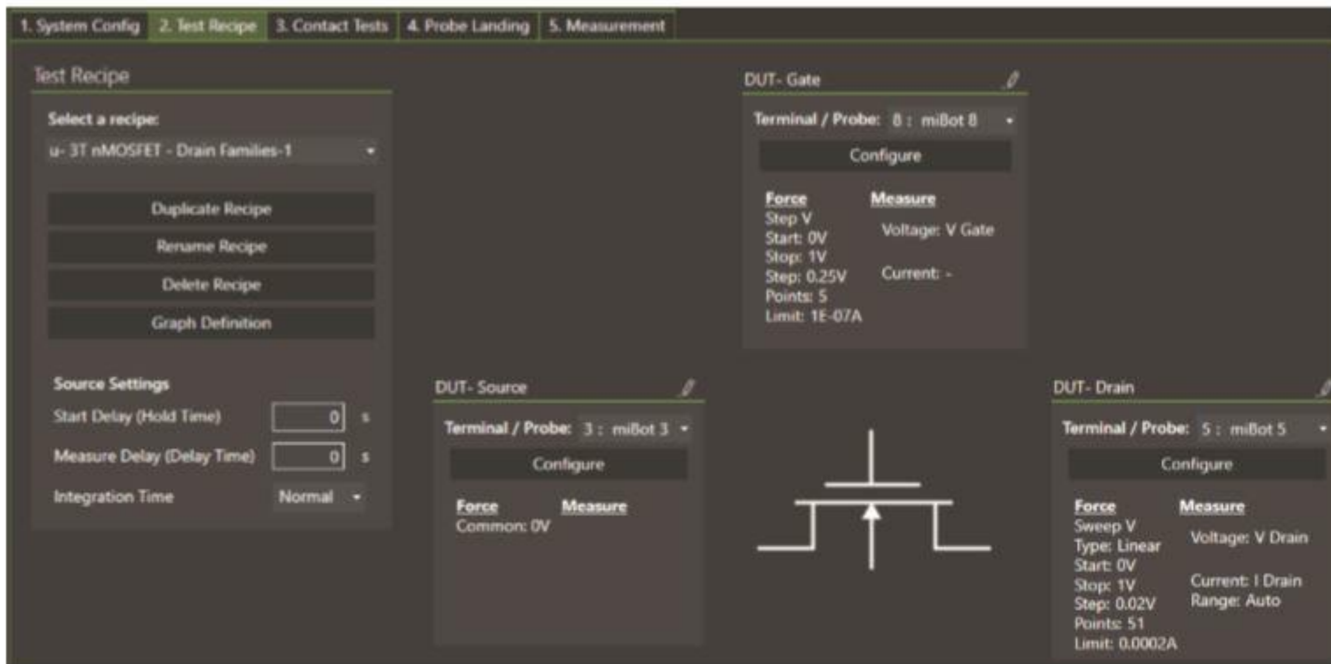
Steps involved in electrical probing



2: Test Recipe

- Predefined test recipes for NMOS and PMOS transistor characterization can be selected.
- Their parameters such as the current compliance, current and voltage range, and number of test points are tuned based on the theoretical properties of the DUT (Device under Test).
- The device used in this case is 3T-nMOSFET.

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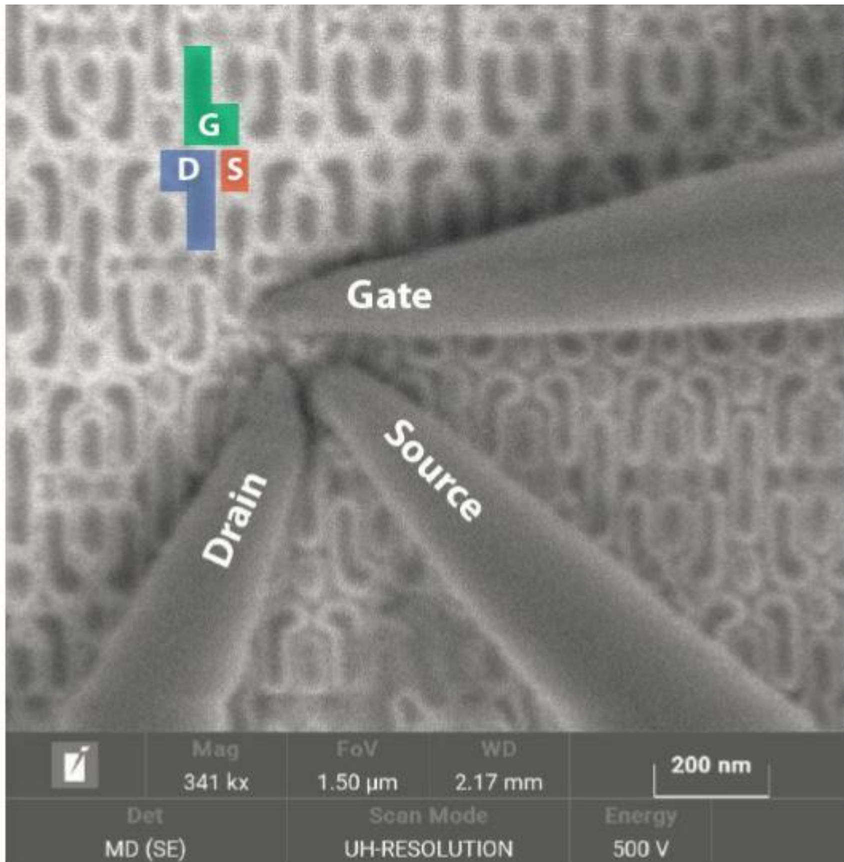
Steps involved in electrical probing



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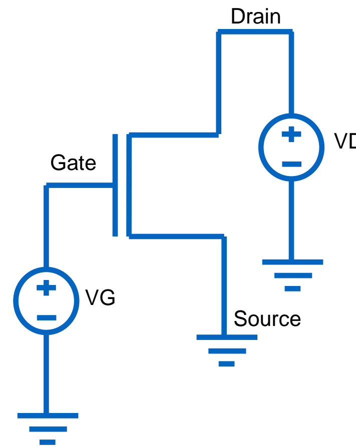

- The probes tips are then sequentially lowered down in contact with each transistor node.
- Switching from one prober to another and adjusting their speed and positioning step size was intuitively done using the control pad.
- Once all probes had touched down, the beam was deflected away from the test area to avoid affecting electrical measurements.

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Steps involved in electrical probing

4: Live Contact Testing

- Precisio™ contact test module was then used to quickly check the quality of electrical contacts by repeating fast measurements.
- When required, probes position was slightly adjusted until measured curves become characteristic of the DUT.

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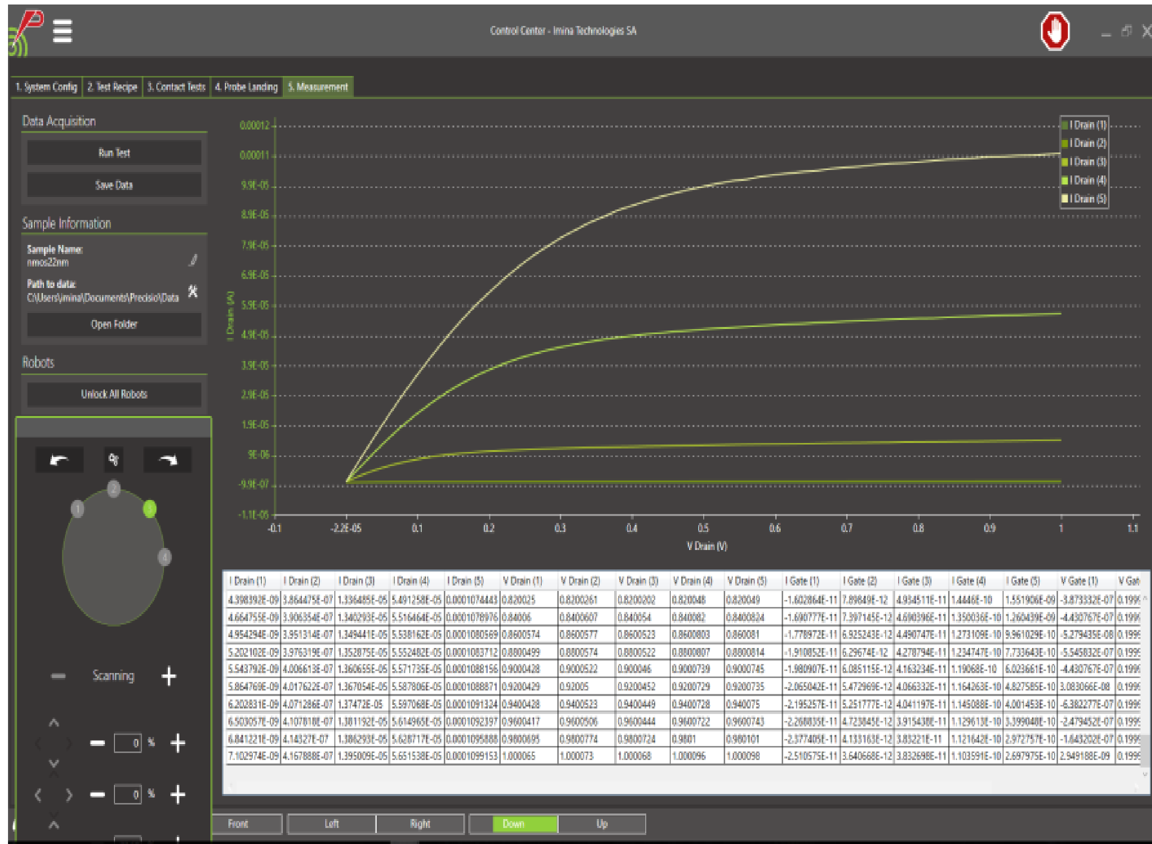
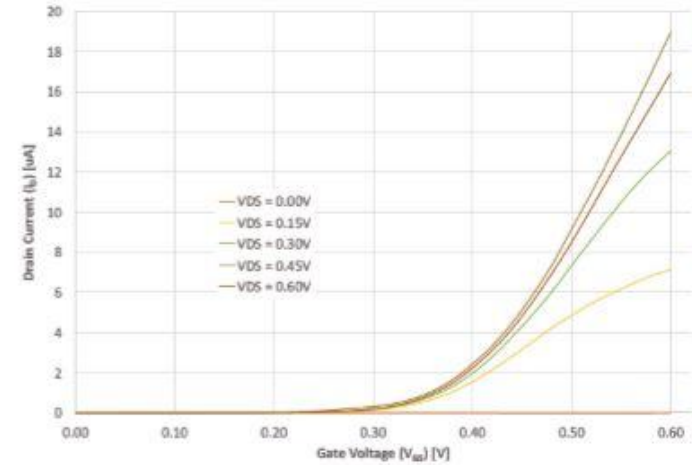
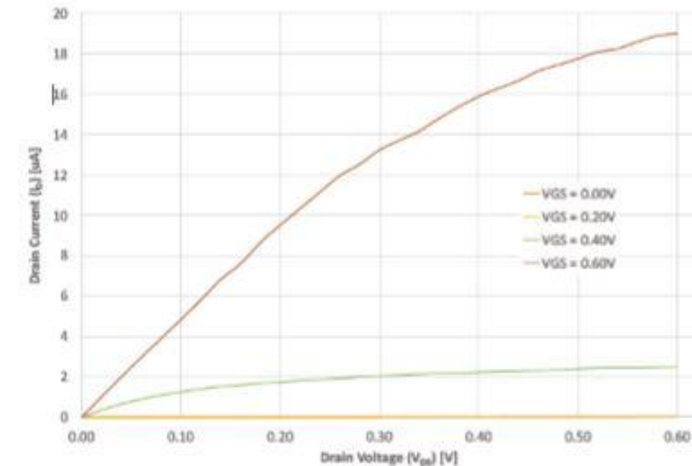
Steps involved in electrical probing



5: Measurement & Report





NMOS transistor characteristics
(Top) Drain current vs Gate-Source voltage sweep
(Bottom) Drain current vs Drain-Source voltage sweep.

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Steps involved in electrical probing

5: Measurement & Report

- Before starting the characterization of transistors, leakage current of each channel was measured when probes were not in contact with the DUT. It was lower than 200 fA on all channels.
- The test recipes for this device were configured with a current compliance on ID and IS set to 100 mA. The Drain and Gate voltage sweeps were made in 31 steps of 0.02 V. The Drain and Gate voltage bias were made in 4 steps of 0.20 V.
- The transistors were characterized by measuring the Drain current ID when sweeping Drain-Source voltage VDS at different Gate-Source voltages VGS (ID=f(VDS)) and when sweeping Gate-Source voltage VGS for different Drain-Source voltages VDS (ID=f(VGS)).
- Source current IS and Gate current IG are also measured.

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