LDO-Based Odometer To Combat IC Recycling

Rabin Yu Acharya[1], Michael Valentin Levin[2], and Domenic Forte[1]
[1]Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA
[2]Honeywell Aerospace, Clearwater, FL USA
Email: rabin.acharya@ufl.edu

***Abstract*—Recycled counterfeit integrated circuits (ICs) are used chips that were removed from discarded electronics and resold in the market as new. Recycled ICs are prone to early failure and serve as a threat to reliability which can be very dangerous if found in critical applications. Although recycled IC detection methods have been researched, there lacks a solution that serves for every chip type and scenario specifically analog and mixed signal (AMS) system-on-chips (SoCs). For example, hardware security primitives have been primarily developed for digital circuits but cannot be directly ported to AMS chips. AMS primitives need to maintain security and reliability along with stringent constraints on area, power, pins, clock, etc. In our prior work, we experimentally studied low-dropout regulator (LDO) aging and resulting power supply rejection ratio (PSRR) degradation. While initial results for standalone LDOs were promising, the results for LDOs embedded in SoCs could be improved. In this paper, we propose a new LDO design which partially re-purposes the already existing LDO in the chip, study its aging effects, and optimize its sensitivity for better recycled chip detection. Since LDOs are often embedded in the power management circuitry in nearly all types of ICs, this solution can function as a lightweight, one-size-fits-all approach for detecting recycled analog/mixed-signal and digital SoCs.**

I. Introduction

Counterfeit electronics is one of the major security and reliability threats in today's era of globalized electronic supply chain. Among the different counterfeit types, recycled and remarked chips account for more than 80% of the total reported counterfeits [1]. Recycled counterfeits are chips that have been maliciously taken off of used and discarded printed circuit boards (PCBs) and inserted back into the supply chain to be sold as new. This causes a major concern for critical system reliability because such chips are prone to faulty and premature failure. With the abundance of AMS and digital ICs in critical systems today, a proportionate rise in counterfeit ICs poses a serious threat to mission success and, in some cases, human lives. By 2030, IHS Markit [2] projects that the number of internet of things (IoT) devices will reach 125 billion; therefore, a commensurate rise in electronic-waste will induce a surge in counterfeit electronics.

To combat the issue of counterfeiting, several methods have been proposed in the literature over the last decade or so. These include the insertion of additional circuitry to detect counterfeits (also called hardware security primitives), electrical tests to compare the parameters of an electronic device to an authentic device, and using advanced imaging techniques to physically inspect the differences between the suspect and authentic chips. Electrical tests and physical inspection are promising techniques but they both require the use of an authentic chip or golden measurements. Similarly, advanced imaging techniques require expensive facilities and expert technical ability to accurately detect the counterfeits. Hardware security primitives on the other hand are quite inexpensive and in most cases do not require the use of a golden IC. However, they have to be meticulously designed and inserted during the design phase of an IC. Earlier works in the design of hardware security primitives include the design of physical unclonable functions (PUFs) which can be used for IC authentication and chip identification [3]. These techniques are mostly used to detect cloned and overproduced ICs. Apart from PUFs, CDIR (combating die and IC recycling) sensors/ odometers have been established as a low cost option for detecting recycled digital ICs in [4], [5]. CDIR is a lightweight structure that measures the frequency degradation in digital circuits through "self-referencing" and uses it to characterize new (authentic) and used (recycled counterfeit) chip. However, these primitives are only applicable to digital ICs. In the case of AMS ICs, counterfeit detection specifically the detection of recycled chips have been hugely understudied. In our previous work [6], we used semi-supervised machine learning approach to detect counterfeit LDOs by comparing them to the vendor specifications. While this approach worked well for stand-alone LDOs, it fails to work as well in the case of LDOs embedded in SoCs. In this paper, we design a new odometer based on LDOs which basically re-purposes the existing LDO inside the SoC and can be used to measure the PSRR degradation instantly to help classify a chip as authentic or counterfeit.

An odometer is an instrument commonly used to measure a distance traversed by a vehicle – this distance can be associated with the vehicles "wear and tear". In the case of recycled IC detection, an odometer is used to measure the distance between an IC's original performance and its current (used) performance. Odometer-based systems have commonly consisted of ring oscillators (RO) to accurately measure frequency degradation due to aging in [7]. In our prior work, we experimentally studied low dropout regulator (LDO) aging and resulting PSRR degradation. LDO is a DC linear regulator found in almost every IC and is used to maintain a stable power supply. PSRR, which is also known as ripple rejection, measures the LDO's ability to prevent the regulated output from fluctuations caused by input voltage variations. We found that the pass transistor of an LDO significantly ages with AC and DC stress and PSRR degradation could be used to detect recycled LDOs [8] and recycled SoCs containing

LDOs [6].

Thus in this paper, we examine a new LDO design with odometer capabilities. More specifically, the contributions of this paper are summarized as follows:

- Design and simulate a low-cost LDO-based odometer that measures the characteristic changes or distance in performance parameters between an aged/used pass transistor (PT) compared to an unused/reference one within the LDO.
- Employ the aging models described in the literature to create a dataset of recycled LDOs that have been aged for different time periods.
- Design a one-class classifier that can accurately distinguish between an authentic and a recycled LDO chip. We also design a linear regression classifier that can accurately predict for how the long the recycle LDO chip has been aged.
- Compare the performance and efficiency of the LDO odometer to a typical LDO.

The rest of this paper is organized as follows. Background information about LDO and transistor aging is presented in Section II. Section III describes the design methodology behind the custom-LDO Odometer. Simulation results and analysis is presented in Section IV. Finally, conclusions are drawn and future work is described in Section V.

II. Background

A. Low Dropout Regulators (LDOs) and PSRR

Low dropout regulators (LDOs) are embedded inside the power management circuitry of practically all ICs to provide a stable voltage for the rest of the circuit. It is a type of DC regulator which maintains an output voltage when the input voltage is very close to the output. It consists of a feedback loop with an error amplifier (EA), a pass transistor (PT) and a resistor divider as seen in Figure 1. The PT behaves as a variable resistor which is controlled by the EA and feedback resister divider to regulate the output voltage. The EA is provided with a fixed voltage reference and monitors the difference between the input and output voltages of the circuit (i.e., V_{in} and V_{out}). It controls the gate voltage of the PT to regulate the output at the stable voltage desired.

Figure 2 shows the operating regions of an ideal LDO. They operate in three different regions: linear region (where the feedback loop regulates V_{out}), dropout region (where the circuit operates with very little feedback), and off region (where the circuit no longer regulates V_{out}). The dropout voltage is the input-to-output differential voltage at which the circuit ceases to regulate against further reductions in input voltage. As long as the operating input voltage is not below the dropout voltage, the output will be regulated with very good stability. One of the major parameter metrics which is used to characterize the performance of a LDO is the power supply rejection ration (PSRR). PSRR measures the ability of suppressing the variations of the input power supply at its output. These variations or ripples can arise from the power supply itself, from the DC/DC converter, or from different intermediate circuits within the system that share the same supply. Equation (1) below shows the mathematical representation of PSRR expressed in decibels or dB.

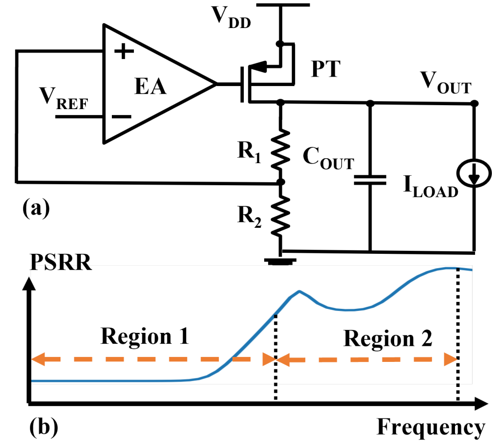

Fig. 1: (a) Diagram of a typical LDO. (b) Curve showing different regions of the PSRR.

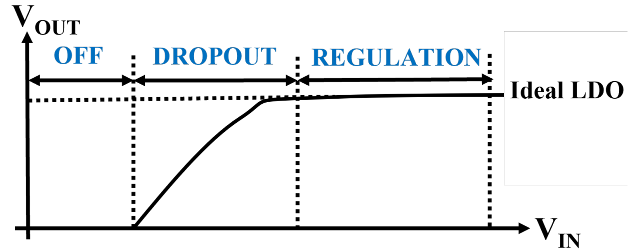

Fig. 2: Typical Regions Of Operation For Ideal LDO

$$PSRR\ [in\ dB] = 20log_{10}\left(\frac{V_{OUT}}{V_{DD}}\right) \tag{1}$$

The PSRR curve of most LDOs can be divided into two distinct regions as shown in Figure 1b: Region 1 which is in the low and mid frequency range and Region 2 located in the higher frequency range. Region 1 is mainly dictated by the DC loop gain of the LDO which comprises of the gain of the EA, the PT, and the resistor divider at the output terminal. Region 2 is however mainly affected by the output capacitor and the intrinsic parasitic capacitance of the input, the output, and the PT [9].

B. Transistor Aging Model

Aging is defined as the change or degradation of the performance of a circuit over time, and is regarded as one of the main causes of reliability issues faced in modern ICs especially for circuits integrated in 65 nm CMOS technology and lower [10]. This phenomena is mostly the result of two different mechanisms that become prominent over time: hot carrier injection (HCI) and bias temperature instability (BTI).

HCI: HCI is caused by fast-moving electrons or carriers which gain enough energy to be injected into the gate after a certain time of use. This creates traps at the silicon substrate and hence results in the degradation of device characteristics such as the threshold voltage (V_{th}). This mechanism has been modeled as a power law dependence on stress time as reported in [11] and

the damage increases exponentially with increasing V_{GS} and V_{DS} as shown in Equation (2) below,

$$\Delta V_{th} \approx \frac{1}{\sqrt{L}} t^{n_{HC}}\ exp(\alpha_3 V_{GS})\ exp(\alpha_4 V_{DS}) \qquad (2)$$

where n_{HC} represents the time exponent, α_3 and α_4 are technology-dependent voltage scaling parameters, and L is the length of the transistor [11].

BTI: BTI is a temperature-activated mechanism and is caused by constant electric fields degrading the dielectric. This in turn traps the hole in the dielectric bulk and degrades the threshold voltage of the transistor. When the device is turned off however the trapped holes are released and the device immediately enters the recovery phase. In a typical device with SiO_2 or SiON dielectric, BTI mainly affects PMOS transistors (i.e., Negative BTI or NBTI). The change in threshold voltage(ΔV_{th}) as a result of BTI can be modeled as Equation (3) below [11],

$$\Delta V_{th} \approx\ exp(\alpha_1 V_{GS})\ t^{n_p} + V_{GS}^{\alpha_2}(C_R + n_R\ log_{10}(t)) \quad (3)$$

where α_1 and α_2 are the voltage scaling factors, n_P and n_R are the time exponents, and C_R is a process dependent capacitance value. Experimentally it has been shown that as the time of device use increases, BTI dominates the effects of HCI for a short period after which HCI causes equal or higher degradation in the device parameters compared to BTI [12].

The two models described here describe the effects in the threshold voltage of the transistor. In the case of LDO, these aging effects can be translated to the effect in the transconductance of the EA and the PT, which mainly affects the Region 1 of the PSRR. This can be considered as one of the limitations of these aging models as they fail to properly model the effects of aging in the Region 2 of the PSRR.

C. Prior Odometers

CDIR based odometers presented in [4], [13] are embedded within digital ICs and use ring oscillators (ROs) to measure the effects of aging by applying a self-referencing concept. Two ROs are embedded very close together inside the chip and their frequencies are compared to detect prior IC usage. One RO is referred to as the *reference RO* and it is designed to not experience stress under normal operating conditions. The second RO is called the *stressed RO* and it is designed to age during normal operating conditions at a much faster rate then the reference RO. As the IC is used in the field, the stressed RO's rapid aging reduces its oscillation frequency while the reference RO's oscillation frequency remains static over the chip's lifetime [4]. Therefore, a large disparity between the ROs frequencies would imply that the chip has been used.

The best CDIRs should possess minimal aging in the reference RO and maximum aging for the stressed RO [4] for improved sensitivity and accuracy. CDIRs are designed in multiple fashions and can be used on a variety of digital ICs to protect against IC recycling. In this paper, we will exploit the self-referencing concept of CDIRs to design a similar odometer for AMS ICs using an LDO with a reference and stressed PTs.

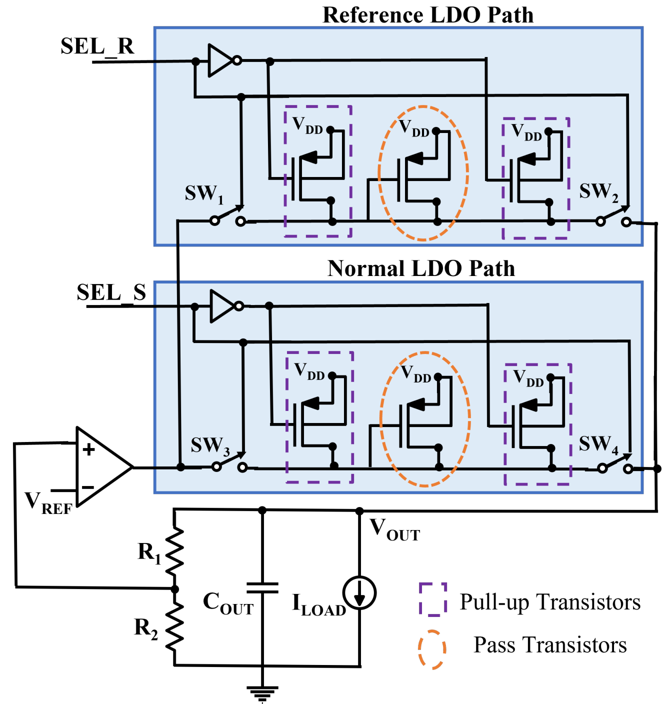

Fig. 3: LDO odometer implemented with stressed and reference paths. Note that a typical LDO would only have the stressed path.

III. Design Methodology

A. LDO Odometer Design

A block diagram of the custom-LDO odometer implemented in 65nm technology is shown in Figure 3. For a normal LDO, the PT can be PMOS or NMOS; however with an NMOS pass element, a charge pump would be required to regulate the voltage. Therefore, a PMOS PT was chosen for a more simple design. Compared to the typical LDO design shown in Figure 1, the custom-LDO contains two distinct feedback PT paths: a reference path and a stressed (normal mode) path. To switch between the two paths, transmission gates serve as high impedance switches (SW1 through SW4) along the gate and drain of both PTs. When SEL_S is 0 and SEL_R is 1, the normal (stressed) path would be selected for DC regulation, while the reference path is in high impedance. SEL_R's complimented signal will also activate the sleep transistors in the reference path to prevent the reference PT from aging (V_{gs} and $V_{\mathrm{ds}} \approx 0$). PMOS sleep transistors are placed at the gate and drain of the reference PT to ensure a low V_{ds} and V_{gs} to lower its stress under normal conditions.

The switches were required to be large enough that the R_{on} of the transmission gate could be as small as possible, i.e., to avoid extra resistance along the PTs drain path towards the load. Depending on how large the impedance is from the PTs drain to the output, a larger dropout region will occur and increase with larger current loads. This can be very critical for voltage stability if the operating voltage is within close proximity of the dropout region or if current loads are higher than expected.

B. LDO Odometer Modes of Operation

To measure both the stressed and reference pass transistors, the custom LDO was intended to function in multiple modes as shown in Table I. First, when the chip is initially fabricated and packaged, both the reference and stressed paths will be at their initial conditions. If the chip is tested post-fabrication and/or test, the *test mode* should be used. Here, the SEL_S and SEL_R are switched between 0 and 1 so that both PTs will then undergo through initial aging for some equal amount of time. This can be accomplished by using a simple oscillator (not shown) that will slowly switch between the normal path to the reference path to allow both transistors to age equally with a 50% duty cycle. When the chip is used in the field, the *normal mode* is used. In this mode, the stressed PT will age from use while the reference PT is put in its low stress condition to avoid aging. Throughout the chip's lifetime, the stressed PT will degrade resulting in the degradation of its threshold voltage. This in turn will heavily impact the LDO parameters specifically PSRR which will shift away from its reference. If a counterfeiter attempts to sell a recycled chip containing the LDO odometer in the market, it can be detected. Upon purchase, the customer can put the chip into *measurement mode* (same as test mode from earlier). Then, by monitoring the changes in parameters for LDO as it switches from stressed to reference paths, the chip can be characterized as authentic (new) or recycled counterfeit (used).

C. Classification of Chip as Authentic or Recycled

A one-label classifier can be trained on different instances of the authentic LDO odometer. This classifier can use the measurements of different LDO chips taken during the measurement mode and classify each chip as authentic or recycled. Similarly, we also train a linear regression based classifier which can predict how long the chip has been recycled or used for. We use Monte Carlo simulation to create different instances of the LDO chip. In addition, we use the transistor aging model described in Section II-B to simulate the effects of transistor aging for different time scenarios. It must be noted that since the aging model describes the change in the threshold voltage of the transistor, this mainly affects the transconductance of the EA and the pass transistor. This means that the aging model can only be used to model the aging effects in the Region 1 of the PSRR. Nonetheless, we age the pass-transistor (PT) and record the corresponding PSRR values for different times. This new PSRR data (or the aged PSRR data) is then used to train the linear regression classifier which when tested on an unseen recycled data can tell for how long that specific chip has been aged for.

IV. Simulation Results

A. Simulation Setup

The netlist shown in Figure 3 is simulated in 65 nm technology node in Cadence ADE-XL environment. As specified in Section III, Monte Carlo simulations were performed to simulate different instances of LDO odometer to mimic different LDO odometer ICs. Figure 4 shows the PSRR values for 100 different chip instances. Then to mimic the effects of aging, the time dependent model described in Section II-B is used to age the pass transistor (highlighted using dashed oval in Figure 3) for different times. Essentially the changes in threshold voltage described in Equations (2) and (3) are used and added together to get the total change in threshold voltage as a result of aging. Then the corresponding PSRR values are recorded to get the aged PSRR values for different aging times. Figure 5 shows the PSRR values for different time stamps for a single LDO odometer chip. As seen in the figure, the shifts of PSRR values are more distinguishable in the lower-to-mid frequency range and that the PSRR values shifts higher as the LDO chip is aged more.

TABLE I: Modes of Operation

Mode	Signals		Description
	SEL_R	*SEL_S*	
Normal Operation	0	1	Stressed PT is aging (Chip is running normally)
Measurement	0	1	Both PTs are aging individually, for the same amount of time.
	1	0	(SEL_R and SEL_S are slowly oscillating at the same rate with complementary phases)

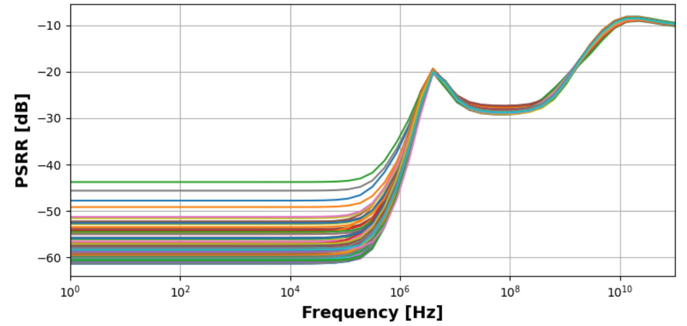

Fig. 4: Graph showing 100 Monte Carlo samples of the authentic LDO odometer chip.

B. LDO Odometer Results and Analysis

Figure 6 shows the voltage characteristics curve at different reference voltages (V_{REF}) for the LDO odometer. This is measured for $I_{LOAD} = 10mA$. In each case, the dropout voltage, which is basically the difference between V_{OUT} and V_{IN} at the point when the regulation starts, is less than $50mV$. Depending on the V_{IN} and V_{OUT} requirements, the designer can choose the corresponding V_{REF}. For the rest of the experiment, we will keep $V_{IN} = 1V$, $V_{REF} = 0.6V$, and $I_{LOAD} = 10mA$.

Comparison of the LDO odometer to a typical LDO: We now compare the performance of the LDO odometer to our previously designed LDO [6] which performs as a typical regular LDO. Figure 7a shows how the LDO odometer maintains the output voltage for loads of up to $590mA$ compared to $210mA$ of the regular LDO. Similarly, Figure 7b compares the quiescent current (Iq) or the ground current of the LDO odometer to that of the regular LDO. Iq is the difference between the input and the output current and is an important factor in determining current efficiency. Basically lower the Iq,

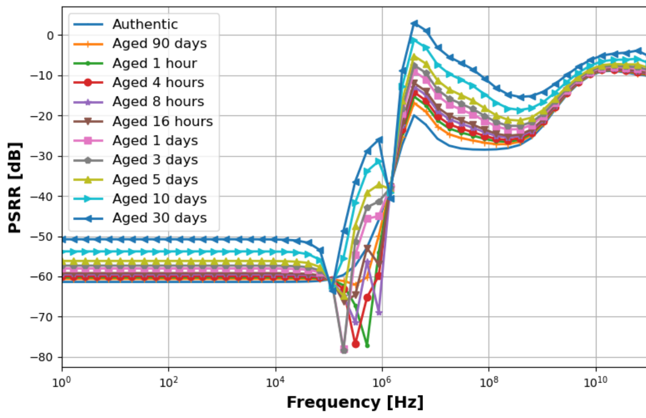

Fig. 5: Graph that shows the authentic and aged PSRR values at different time stamps of a LDO odometer chip.

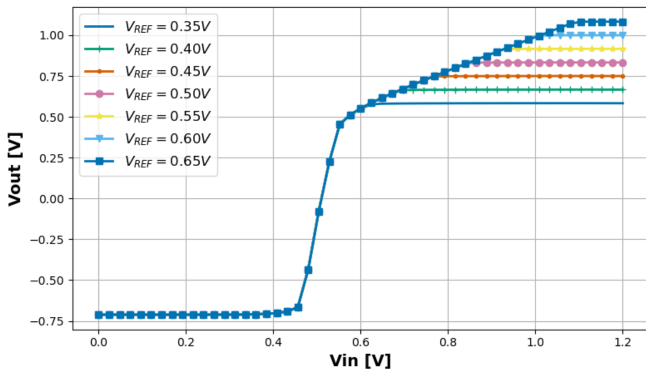

Fig. 6: Vout versus Vin characteristics for different V_{REF} voltages.

higher the efficiency is. And as seen in Figure 7b, the regular LDO is much more current efficient than the LDO odometer. These results are summarized further in Table II.

C. Classifier Training

We then train the two classifiers as described in Section III-C: a one-label classifier to classify the chip as either authentic or recycled (aged), and a regression classifier that calculates for how long the recycled chip has been aged.

Training the one-label classifier: For this purpose, we use the one-class SVM with a radial basis function (RBF) kernel [14]. We chose support vector machines (SVM) as our classification algorithm because they are quicker and more effective when considering limited number of training samples. Similarly, for the kernel function we chose the RBF kernel as it is one of the most widely used kernel functions and is shown to be

TABLE II: Comparison of the LDO metrics between the regular LDO and the LDO odometer.

LDO metrics	Regular LDO	LDO odometer
PSRR @ 50 kHz	-58.835 dB	-61.379 dB
Iq @ Load = 0mA	10 μA	8 μA
Nominal Vout	1 V	1 V
Dropout voltage	53 mV	47 mV
Current efficiency	99.8 %	97.6 %

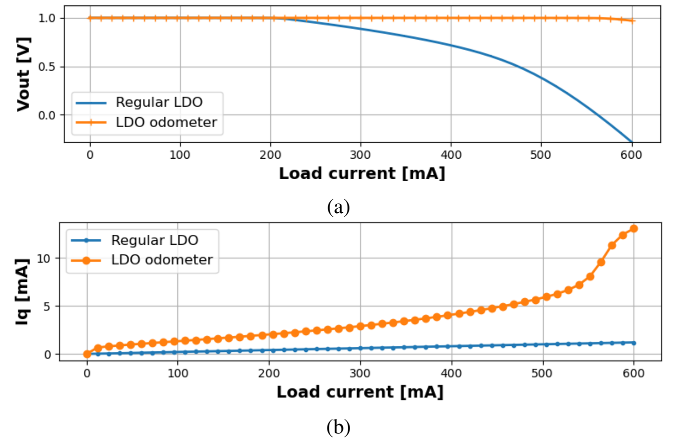

Fig. 7: Comparison of the (a) load regulation and (b) quiescent current between the regular LDO and the LDO odometer.

TABLE III: Table showing different times used to age the LDO odometer.

Time stamps					
	1 hour	4 hours	8 hours	16 hours	1 day
	3 days	5 days	10 days	30 days	90 days

quite effective in computing the similarity between two sample points. The dataset is comprised of both authentic samples and the aged samples; however, the classifier is trained using only the authentic PSRR samples. The authentic PSRR samples are comprised of 1000 Monte Carlo samples of the authentic LDO odometer chip. For testing, the combined dataset that consists both authentic and aged samples equally is used. The aged samples are generated using the time-based aging model as described in Section III-C.

Training the linear regression classifier: For this purpose, we use the default linear regression model provided by scikit [14]. The model is trained on a total of $10,000$ aged samples (1000 samples for each of the timestamps shown in Table III generated by aging the 1000 Monte Carlo samples of the LDO odometer). Each sample is labeled by its corresponding timestamp.

D. Classification Results

Results of the one-label classifier: The results and performance of the one-label classifier is summarized in the receiver operating characteristic (ROC) curves drawn in Figure 8. The higher the area under the curve, the higher the performance/accuracy of the classifier for that dataset. A ROC curve basically illustrates the ability of the classifier to distinguish between an inlier (belongs to the one-class) and an outlier (does not belong to that one-class) at all classification thresholds. In our case, the thresholds are the 10 different increasing timestamps mentioned above and shown in Figure 8. As can be seen from the figure, the area under the ROC curve increases as the thresholds are increased indicating that the classifier is able to detect outliers very clearly. The area is lower in the case of 1 hour aged samples because the LDO odometer has not been aged long and the shifts in PSRR

TABLE IV: Accuracy and F1 score of the one-class SVM classifier. Each dataset consists of an equal number of samples of authentic and aged samples.

Dataset	F1 score	Accuracy
Authentic + Aged 1 hour	0.30	0.57
Authentic + Aged 4 hours	0.51	0.66
Authentic + Aged 8 hours	0.68	0.75
Authentic + Aged 16 hours	0.82	0.84
Authentic + Aged 1 day	0.89	0.90
Authentic + Aged 3 days	0.96	0.96
Authentic + Aged 5 days	0.98	0.98
Authentic + Aged 10 days	0.98	0.98
Authentic + Aged 30 days	0.98	0.98
Authentic + Aged 90 days	0.98	0.98

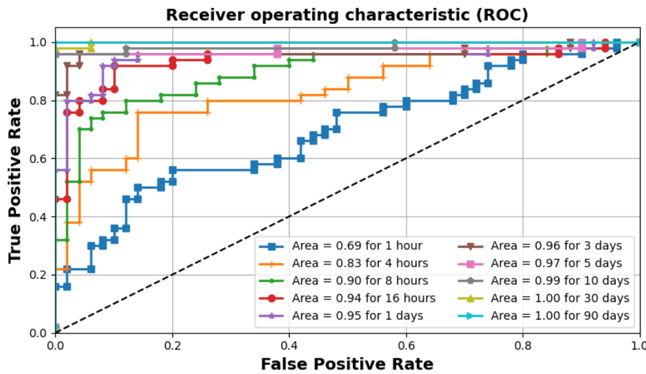

Fig. 8: ROC curves using the one-class SVM classifier against different datasets. Each dataset consists of equal number of authentic and recycled samples. The recycled samples are aged for the corresponding time shown in the legend of the graph.

is not as drastic for it to be easily discernible. The PSRR shift observed in one instance of the LDO odometer chip as a result of aging looks similar to the shift observed as a result of the manufacturing variations (see Figure 4 which shows different instances of the authentic LDO odometer). The accuracy and F1 score of the one-label SVM classifier are summarized in Table IV, and as expected the accuracy increases as the time aged increases.

Results of the linear regression classifier: To assess the performance of the linear regression classifier, we use the mean squared error (MSE). MSE is basically calculated as the average of the squared differences between all predicted and expected target values in the test dataset. The lower the MSE, better the performance of the regression model is. In our case, the MSE value is 7.048 hours.

V. Conclusion and Future Work

In this paper, we presented the first of its kind, a LDO based odometer which can be used to detect counterfeit recycled ICs and SoCs. The capability to compare the aged LDO to its own authentic or reference counterpart makes this approach more robust compared to our previous approach in [6] where even with the use of golden ICs the counterfeit detection accuracy was limited especially in the case of LDO embedded in SoCs.

All work was done in simulation during the pre-layout stage where parasitic extraction was not conducted. In the future, we plan to further improve this design with the use of internal capacitive switching to toggle between SEL_R and SEL_S similarly to [15]. This will be done to prevent the attacker from having precise control over the amount of time that the reference PT ages. If the attacker gets control over the select signals, they can force the reference PT to age the same amount as the stressed one. We also envision the custom-LDO odometer to be fully operational in a SoC without the use of external pins. Finally, we would like to develop a modified odometer that does not require any external equipment for measurement.

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