Aging Analysis of Low Dropout Regulator for Universal Recycled IC Detection

Sreeja Chowdhury, Haoting Shen, Beomsoo Park, Nima Maghari and Domenic Forte

***Abstract*— Recycled counterfeit integrated circuits (ICs) are previously used chips that originate from improperly disposed electronics (i.e., e-waste) and are then sold in the market as new. Recycled ICs are dangerous and prone to early failure due to mishandling and deterioration from prior use. With the number of IoT devices expected to reach 125 billion in 2030, e-waste and therefore recycled ICs will face a commensurate rise. Although recycled IC detection and avoidance methods have been emerging over the last decade, there still lacks an all-in-one solution. Previously, we discovered low dropout regulator (LDO) aging can be detected with high confidence by measuring the LDO's power supply rejection ratio (PSRR). Since LDOs are embedded in the power management circuitry of virtually all ICs, our method could be applied to avoid recycled chips in any IoT setup, thus bolstering IoT security. Since commercial LDO designs are proprietary to individual design houses, it is difficult to determine the most important sources of degradation. Thus, in order to study this phenomenon further, we have fabricated a custom design generic LDO in 65nm process. Our analysis in this paper reveals ways to improve counterfeit IC detection based on LDOs as well as to develop LDO designs that are even more sensitive to aging/use.**

I. INTRODUCTION

State-of-the-art discoveries in computing, vision, artificial intelligence (AI) and electronics have constructed a smart world where every electronic component of daily use are connected to each other though internet. This creates a mesh of connected smart components called Internet of Things (IoT). Apart from all the advantages offered to mankind, the ubiquitous nature of IoT devices induces several security concerns. If even a single component in these connected smart electronics is unreliable and counterfeit, the security and reliability of the entire IoT system can be put in jeopardy. According to IHS Markit [1], the number IoT devices is expected to reach 125 billion by 2030. The extraordinary increase will induce a proportionate surge in counterfeit electronics, especially recycled integrated circuits (ICs). Recycled ICs are prior used ICs originating from improperly disposed electronics (e-waste) which are sold as new in the market by untrusted suppliers. They exhibit deteriorated performance and shorter lifespan due to prior use and mishandling. The presence of a recycled IC can render an IoT or industrial control system unsafe.

Different categories of counterfeit ICs have been shown in [2]. Prior work in counterfeit detection include new design implementations like physical unclonable functions (PUFs) which are capable of detecting cloned and overproduced ICs. The basic idea of silicon PUFs was first given by Gassend et. al in [3]. After that, different types of PUFs have been devised for authentication of ICs and key generation purposes. Apart from implementation of PUFs in digital ICs, recent research articles have also concentrated in analog and mixed signal (AMS) PUFs as can be seen in [4]. Apart from PUFs, low-cost on-chip structures called CDIRs (combatting die and IC recycling) have been demonstrated in [5]. Silicon odometers which can accurately measure frequency degradation in digital circuits have been proposed in [6]. Compared to digital ICs, counterfeit detection and avoidance has been studied less in AMS circuits. The challenges and opportunities related to detection and avoidance of analog counterfeits have been enlisted in [7]. In this paper, we propose to observe the PSRR degradation of an LDO, a component indispensable in any IC (digital and AMS), thus bolstering counterfeit detection in digital and AMS ICs.

In our prior work, we have investigated commercial-off-the-shelf LDOs from different vendors. After accelerated aging, machine learning algorithms were able to detect aged LDOs with high accuracy [8]. LDOs are DC linear regulators which are extensively used to maintain a stable power supply in almost every IC, including system on chip (SoC). PSRR is the capability of an LDO to suppress supply voltage ripples and provide a clean and stable output. In order to stabilize the operation of an LDO, it's output is often connected to a external capacitor thus making it easy to access. Our experimental results showed that the PSRR of an LDO degrades with use/transistor aging. Since, industrial LDO designs are proprietary, we further analyze the degradation of the PSRR curve with a custom designed LDO in 65nm process. Our contributions are as follows:

- Analysis of degradation of PSRR metric of LDO, due to transistor aging in two regions of operation. We identify the most critical design element and source of degradation as the LDO's pass transistor (PT).
- Analysis of degradation of PT parameters including current voltage curves and their influence on the PSRR.
- Validation of our analysis in simulation and silicon. PSRR measurements are taken from custom LDOs (65nm) before and after artificially aging using DC (NBTI) and AC (HCI) electrical stress.

The paper is organized as follows: Background material about LDO and transistor aging is presented in Section II. Section III describes the theoretical analysis behind LDO aging degradation. Experimental data and analysis is presented in Section IV. Lastly, conclusion with future work and Acknowledgement comprise Section V and VI respectively.

II. BACKGROUND

A. LDO Operation and PSRR

An LDO is a type of DC linear regulator which maintains an output voltage when the input voltage is very close to the output (i.e., low drop-out). Drop-out voltage of an LDO is defined as the difference of the input and the output voltage when the LDO is incapable of regulating the output voltage, unless the input is further lowered. In Figure 1, the block diagram of an LDO is shown. It consists of an error amplifier (EA), a pass transistor (single NMOS or PMOS) and a resistor divider connected in a feedback loop.

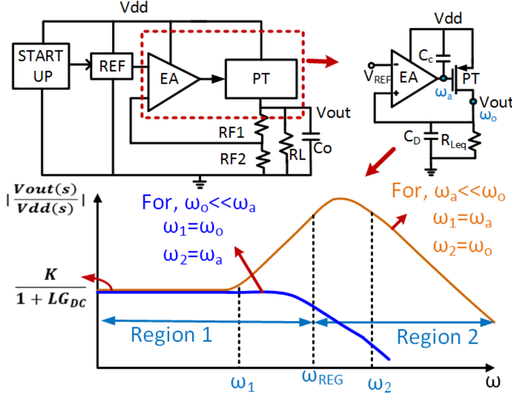

Fig. 1: LDO block diagram with PSR (linear scale) curve [9]

A bandgap circuit or an external voltage maintains a fixed reference voltage (REF) to the EA. The EA controls the gate voltage of the pass transistor (PT) which acts as a variable resistance. The EA continuously monitors the output voltage and computes the error between the output and the voltage fed back to it by the resistor divider. If the feedback voltage is smaller, the v_{gs} of PT is increased, raising the current flowing through the PT; thus increasing output voltage and vice verse. The drop-out voltage for a generic LDO as shown in Figure 1, is actually the drain to source voltage drop (v_{ds}) which appears across PT. Since LDOs provide a regulated stable output voltage to isolate the output from the input supply glitches, they are ubiquitous in the power supply of most analog, mixed signal, and digital ICs, including SoCs. PSRR of an LDO is defined as the capability of an LDO to reject input supply ripples at the output. The ripple can originate from the power supply, from a DC/DC converter, or even due to sharing an input supply between different circuit blocks in a system. Mathematically, $PSRR = 20\log(\frac{v_{out}}{v_{in}})$ where, v_{out} and v_{in} are magnitudes of voltage glitch at output and input, respectively.

B. Transistor Aging

Transistor aging is one of the major causes of reliability issue faced by modern ICs. *Bias temperature instability (BTI)* results in a positive shift in the absolute value of threshold voltage V_{th} in both PMOS and NMOS. It is the condition often referred to as DC stress since the PMOS/NMOS has already pulled up/down but the gate is biased in strong inversion. The drain to source voltage becomes zero, signifying negligibly small lateral electric field. For PMOS, the condition is called negative BTI (NBTI) whereas for NMOS it is positive BTI (PBTI). *Hot carrier injection (HCI)*, also referred as AC stress, occurs when the transistor is switching under strong inversion ($|v_{gs}| \approx V_{dd}$) and the lateral electric field is high ($|v_{ds}| \approx V_{dd}$). During transistor switching, the accelerated carriers drift towards the drain under the influence of the lateral electric field. Channel hot carriers (CHC) are generated when the source to drain current flowing though the channel reaches an energy above the lattice temperature. These hot carries gain energy and get injected into the gate oxide, forming charge traps. As a result, parameters such as V_{th}, transconductance, and saturation current of transistor are shifted [10].

We have chosen the LDO as our main component because of its universal presence in most ICs. In other words,

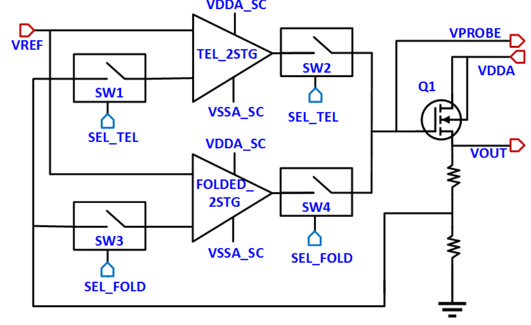

Fig. 2: Block diagram of LDO fabricated in 65nm process

PSRR degradation due to transistor aging can aid recycled counterfeit detection of any chip/SoC. An analytic model of LDO aging degradation will help in comprehending the complex aging process. In [11], the authors characterize the HCI aging effect on different parameter metrics of a simple LDO to improve yield but they do not focus on the aging effect on PSRR. In contrast, our paper focuses exclusively on the degradation of LDO PSRR to aid in counterfeit detection.

III. Analysis of Aging on LDO PSRR

A. PSRR Transfer Function

Figure 1 shows the block diagram of a generic LDO. whereas in Figure 2, the block diagram of the LDO implemented in 65nm is shown. The LDO implementation consists of two different opamps (folded-cascode and telescopic) in order to analyze design dependent aging effects. The switches SW1 through SW4 are used to select which opamp is used in the feedback loop. In order to understand the effect of transistor aging in LDOs, one needs to examine the transfer function of the PSRR. Referring to the generic block diagram of an LDO in Figure 1 and the explanation given in [9], the power supply rejection of a generic LDO, i.e., *PSR* (in linear model), can be represented as

$$PSR = \frac{v_{out}(s)}{v_{dd}(s)} = \frac{K(1+\frac{s}{\omega_a})}{(1+\frac{s}{\omega_a})(1+\frac{s}{\omega_o})+A_aA_o} \quad (1)$$

$$= \frac{K}{(1+\frac{s}{\omega_o})(1+LG(s))} \quad (2)$$

where,

$$LG(s) = \frac{A_aA_o}{(1+\frac{s}{\omega_o})(1+\frac{s}{\omega_a})} \quad (3)$$

$$K = \frac{R_{Leq}}{R_{Leq}+r_{dsP}}, \quad \omega_a = \frac{1}{ro_{ea} * C_c}, \quad \omega_o = \frac{1}{(r_{dsP}||R_{Leq}) * C_D}$$

$$A_a = g_{ma} * r_{oa}, \quad A_o = g_{mP}(r_{dsP}||r_{out}), \quad ro_{ea} \propto \frac{1}{I_D} \quad (4)$$

$$g_m \propto v_{eff}, \qquad v_{eff} = v_{gs} - V_{th} \quad (5)$$

LG is the feedback loop gain of the LDO, r_{dsP} refers to the drain to source small signal resistance of PT while r_{oa} is the small signal output resistance of the amplifier. || denotes parallel configuration. The equivalent output resistance at the node v_{out} is taken as r_{out}. The error amplifier and the pass transistor have respective transconductances of g_{ma} and g_{mP} and loop gains A_a and A_o.

Since, PSRR is the measure of how well the LDO is capable of rejecting the noise in V_{DD} at it's output, the

performance of the transistors connected to V_{DD} is critical. The PT is one of the major transistors connecting the V_{DD} and is also very large in size compared to other transistors. Any degradation in PT due to transistor aging affect the PSRR directly. Apart from the PT, the gain-bandwidth of the EA also affects the PSRR. Decrease in the bandwidth due to transistor aging can also be distinctly detected in the PSRR curve.

The PSRR curve of most LDOs can be divided into two distinct regions (see Figure 1). The first one (region 1) occurs in the low and mid frequency range till the unity bandwidth frequency (ω_{reg} where the DC loop gain becomes 1) of the LDO regulator. The second region (region 2) is in the higher frequency range located after the regulator bandwidth frequency. In region 1, the DC loop gain comprising of the individual gain of the EA, PT and the feedback ratio (resistor divider) mainly controls the PSRR value till the dominant pole (ω_1). After that, the loop gain reduces and at the unity bandwidth frequency (ω_{REG}) in Figure 1, the loop gain reaches unity at the end of region 1. In Figure 2, for the implemented LDO (65nm process), as we have Tgate switches connecting the EA to the PT, the definition of the pole at ω_{a} changes slightly. The resistance at the gate of PT translates to the equivalent resistance looking into the source of the MOS transistors of Tgates. The capacitance C_{c} in Figure 1 thus translates to the sum of the gate capacitance C_{g} of the PT, the source capacitances of the PMOS and NMOS of the Tgate switches SW2 and SW4 ($C_{\mathrm{s_{swp}}}$ and $C_{\mathrm{s_{swn}}}$), and the capacitance due to the pad at Vgate:

$$C_{\mathrm{c}} = C_{\mathrm{g_{PT}}} + 2 * (C_{\mathrm{s_{swp}}} + C_{\mathrm{s_{swn}}}) + C_{\mathrm{pad}} + C_{\mathrm{w}} \tag{6}$$

$$C_{\mathrm{d}} = C_{\mathrm{d_{PT}}} + C_{\mathrm{o}} + C_{\mathrm{pad}} + C_{\mathrm{w}} \tag{7}$$

The other capacitance C_{D} is equal to the sum of the equivalent drain capacitance C_{d} of PT, the equivalent output capacitance C_o (located off-chip), the pad capacitance and wire capacitance: In Figure 1, the pole due to the node capacitance (C_{c}) at the output of the error amplifier originates at frequency ω_{a} while the one due to the equivalent output capacitance (C_{D}) at the output node originates at ω_{o}. As the combined capacitance at the output of the LDO including the output capacitance C_{o} of the PCB is high, we consider ω_{o} as our dominant pole. R_{Leq} is the equivalent resistance at output. Alteration of any of these capacitances, specifically the gate and drain capacitances of the PT can change the PSRR values at higher frequencies. We have found such examples of degradation of capacitances due to electrical stress in literature [12] as well as in our experiments as explained further on in our paper. The individual gain of EA and PT again depends on the transconductance of the EA (g_{ma}) and the PT (g_{mP}). Thus, degradation of the transconductances due to transistor aging can effect the PSRR in region 1. In region 2, the loop gain has little effect and the PSRR is dominated by parasitics from input to output, the output capacitor, PT parasitics, and the PCB. We discuss the aging effect on PSRR over region 1 and 2 in detail in the next section.

B. Aging Effect on PSRR in Region 1

The PSRR (in dB) is shown as negative in Figure 1 and thus implies suppression of output ripples. The more negative the PSRR is, the better the ripple suppression. As discussed earlier, the PSRR in region 1 is actively controlled by the loop gain (LG in Eqn. (2)). As LG decreases after the dominant pole, the PSRR also starts decreasing. Thus higher the LG, better the PSRR. LG is the product of the individual loop gain of the EA and PT and, thus, is directly proportional to the individual transconductances g_{m} as shown in Eqns. (1) and (4).

TABLE I: Summary of parameter degradation of LDO and effect on PSRR

Parameters degrading	**Increasing / Decreasing**	**Possible impact on PSRR**
V_{th}	Increases	Region 1&2: Effects most of the parameters below
I_{D}	Decreases	Region 1&2: Effects most of the parameters below
R_{DS}	Increases	Region 1: Reduces g_{m} Region 2: Shifts pole-zero positions.
v_{eff}	Decreases	Region 1: Reduces g_{m}
g_{m}	Decreases	Region 1: Reduces LG and Bandwidth of EA
LG	Decreases	Region 1: Reduces DC value of PSRR
Bandwidth of EA	Decreases	Region 1 : Shifts position of ω_{REG} to lower frequencies
C_{c}	Increases	Region 2: Degrades PSRR at higher frequencies and shifts position of non-dominant poles/zeros.
C_{d}	Increases	Region 1: Shifts position of dominant pole (ω_{o})
ro_{ea}	Increases	Region 2: Shifts non-dominant pole (ω_{a})

Degradation of g_m: In [13], the authors represent an aging model for the transconductance degradation of MOSFETs as shown in equation below.

$$g_{\mathrm{m}}(t) = g_{\mathrm{o}}(t) - \Delta g_{\mathrm{m}}(t) \tag{8}$$

$$\Delta g_{\mathrm{m}}(t) = g_{\mathrm{o}} \left(\frac{\Delta R_{\mathrm{DS}}}{R_{\mathrm{DS}}} - \frac{\Delta I_{\mathrm{GS}}}{I_{\mathrm{GS}} - I_{\mathrm{GSO}}} \right) \tag{9}$$

where g_{o} is the initial tranconductance, R_{DS} is the drain to source resistance, I_{GS} is the gate to source current and I_{GSO} is the gate to source leakage current with drain open. The degradation in g_{m} can be attributed to the degradation in R_{DS} and also due to the increase in leakage current with transistor aging.

$$\Delta R_{\mathrm{DS}}/R_{\mathrm{DS}} = \Delta \rho_{\mathrm{DS}}/\rho_{\mathrm{DS}} = \Delta l_{\mathrm{DS}}/l_{\mathrm{DS}} \tag{10}$$

The degradation in R_{DS} is represented in the above equation. It occurs due to the scattering inside the inversion channel. ρ is the resistivity and l is the mean free path the electrons travel in channel in between collisions. l increases with transistor aging due to the increment in the defects in the inversion channel due to scattering.

Thus degradation of transconductance plays an important role in PSRR degradation in region 1. It effectively reduces the overall LG and thus the DC value of PSRR in region 1. In some cases, it also degrades the gain bandwidth of the EA thus degrading the PSRR further.

C. Aging Effect on PSRR in Region 2

In region 2, after the LDO unity gain bandwidth frequency, $LG = 1$, the PSRR curve behaves mainly as a resistor divider K in Eqn. (1). In this region, the LG has no impact and the PSRR curve is controlled by the parasitics. The major parasitics include C_{c} and C_{d} (see Eqs. (6) and (7)). C_{d} being the capacitance forming the dominant pole depends on the output impedance of the LDO and the output capacitor. The value of C_{c} decides the position of the non-dominant pole, thus has a significant role in the PSRR curve in region 2. At higher frequencies, C_{c} acts like a short circuit and couples the noise from V_{DD} to the gate of the PT thus degrading PSRR. Electrical stress, specifically HCI, can induce changes in the gate, source and drain parasitics of the PT. The change in parasitics along with the degradation of R_{DS} can shift the poles along the PSRR curve (see Eqns. (4), (6) and

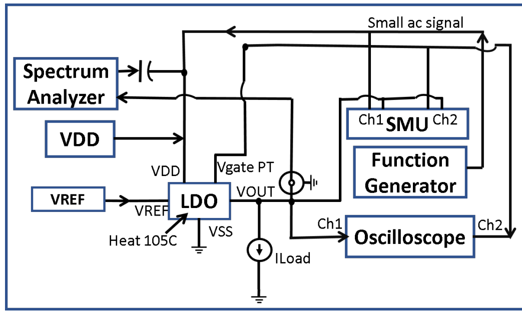

Fig. 3: Block Diagram showing measurement setup for: PSRR, I-V characteristics of PT and phase shift at gate and drain of PT with electrical stress

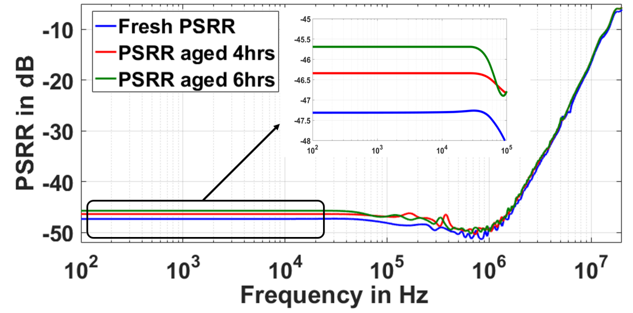

Fig. 4: Silicon results showing PSRR aging degradation owing to DC stress at 105°C using thermostream for 4hrs and 6hrs respectively with 10% increase in V_{DD}. Data recorded after cooling the chip to 25°C with thermostream.

(7)). This phenomena of variation in gate capacitance (C_{gd} and C_{dg}) with respect to hot carrier degradation has been exemplified for a 64-Mb DRAM chip in [14] where electron beam probing was used to detect the difference in gate capacitance before and after hot-carrier stress. Their experimental results showed that the precharge time of the DRAM chip increased from 20ns to 22ns after a 47 hour hot carrier stress, thus exhibiting significant change in gate capacitances. The degradation of all the parameters explained above and their impact on the LDO PSRR has been formulated in Table I.

IV. Experimental Setup and LDO Aging Data

As transistor aging models are foundry specific and not easily obtained, we mainly rely on experimental data depicting the aging of the PSRR. The experiments are carried on four LDO chips (referred to as Chip 1 to Chip 4) fabricated in 65nm technology. DC stress is applied on Chip 1 and Chip 2 to check effect of BTI whereas a combination of AC and DC stress is given to Chip 3 and Chip 4 to check effect of HCI coupled to BTI. The block diagram of the experiments are shown in Figure 3.

A. DC Stress Effect on PSRR of LDO

During the DC stress, the LDOs are placed under a thermostream (Temptronic ATS 605-C) at 105°C while operating with a load current of 1mA and maintaining 1V at its output with an input supply voltage (V_{DD}) of 1.32 V (10% increase over the normal supply voltage of 1.2V). The reference voltage applied to the EA is maintained at 0.6V. According to [15], this stress produces a voltage acceleration factor (V_{AF}) of 0.3 and a temperature acceleration factor (T_{AF}) of 61. Thus, we estimate the total aging acceleration as ($V_{\mathrm{AF}} * T_{\mathrm{AF}}$) $\approx$ 18.3. Thus, 6 hours of aging relates to approximately 5 days of real-time aging. A noise signal with an amplitude of -10dBm generated using the tracking generator of RIGOL DSA815-TG spectrum analyzer, is coupled to the V_{DD} input of the chip. The power spectrum of the LDO output is recorded with the spectrum analyzer. After subtracting the given input power spectrum (originating from tracking generator) from the output power spectrum we obtain the PSRR curves. The initial PSRRs of fresh ICs are recorded over all the LDO chips before applying any kind of thermal or V_{DD} stress. During the initial data recording the temperature is kept constant at 25°C (room temperature) with the thermostream. After that, DC stress is applied to the LDOs (Chip 1 and Chip 2) maintaining the thermostream air temperature at 105°C. After 4 hours of DC stress, the temperature is brought back to 25°C and the V_{DD} is set to normal 1.2V. The chip is allowed to run in normal condition for 10-15 mins and after the temperature settles down, the aged PSRR data is recorded. To remove noise, both initial and aged data recordings are repeated 5 times to compute their means. The silicon chip measurements showing PSRR degradation with 4 and 6 hours of DC stress are shown in Figure 4. With 4 hours of DC stress, the DC PSRR of the LDOs degrade by approximately 1 dB and an additional 2 hours of aging increases the difference of aged and initial PSRR to 1.6 dB. This difference of the DC PSRR in region 1 can be attributed to the change in V_{th}, R_{DS}, g_{m} which cumulatively reduce the individual gain of the opamp and the PT, thus reducing the *LG*. This phenomena is described in detail in Section III-B with all the aforementioned factors contributing to PSRR degradation. *It must be noted that the aging data only pertaining to the LDO loop comprising of the folded cascode opamp and PT is shown as we observed that both the opamps behaved similarly with transistor aging.*

B. DC Stress Effect on Pass Transistor I-V Curve

To further understand the effect of DC stress on the LDO PSRR, we also characterized the I-V characteristics of the LDO's PT before and after stress. The custom designed LDO was provided with an additional pad connected to the gate of the PT. Thus, we had access to drain (V_{OUT}), source (V_{DD}) and gate of PT as seen in Figure 2. While characterizing the PT, we used the Summit 12000B Semi-Automated Probe-Station. The DC stress is applied by increasing the temperature of the probe-station chuck (on which the chip is kept using vacuum suction) to 85°C. We kept the temperature low as the bare die was directly being heated without any packaging. The initial I-V results were obtained by placing probes on the three terminals and recording the data using a Keithley 2600B source meter unit (SMU) (refer: Figure 3). The post-layout simulation results and experimental results representing the initial $I_{\mathrm{source}} - V_{\mathrm{gs}}$ are shown in Figures 5 and 6 respectively. The cutoff V_{GS} for both the simulation and experimental results was approximately 0.3V.

The PT in the above setup was aged by applying a V_{DD} of 1.32V at its source terminal, 0.7V at the gate (replicating the approximate gate voltage obtained from simulation results during the operation of the LDO), and 1V at the PT drain (replicating the LDO output). In this way, we emulated the PT aging during LDO operation using probes. As shown in Figure 6, the aged chip current is generally lower than the fresh chip current. Compared to the fresh I-V curves,

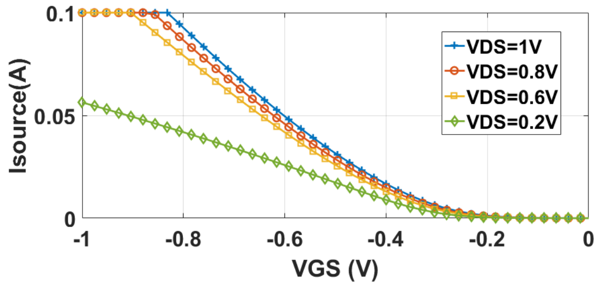

Fig. 5: Post layout simulation results showing IDS-VGS curve of the PT for different VDS (0.2V, 0.6V, 0.8V, 1V)

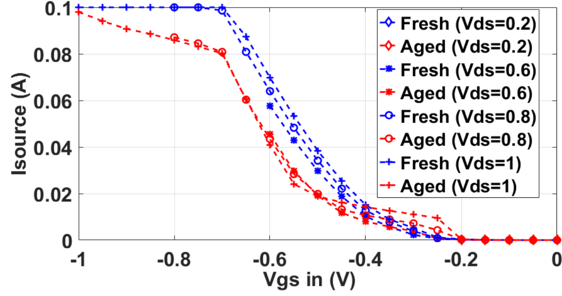

Fig. 6: Silicon results showing IDS-VGS curve of the PT for different VDS (0.2V, 0.6V, 0.8V, 1V) before and after DC stress at 85°C for 6 hours with V_{DD} increased by 10% and cooling to 25°C during data collection. Blue refers Fresh IC; Red refers Aged IC

the aged ones are shifted toward more negative voltages, indicating an increased threshold voltage (V_{th}), which can be explained by the NBTI (DC stress) effect. When V_{ds} is 0.8 V or above, the energy barrier between source and drain is narrowed. In such situations, the trapped charges and defects in the gated oxide make the tunneling leakage higher in the aged device than the tunneling leakage in the fresh device. Given $V_{\mathrm{gs}} \leq V_{\mathrm{th}}$, such tunneling leakage current results in higher Ids in the aged device (as shown in Figure 6, when $V_{\mathrm{ds}} \geq 0.8V$, Vgs is below 0.4V). The increase in the leakage current and the change in V_{th} can affect the R_{DS} and thus the g_{m} as seen in Eqns. (9).

C. Combined DC and AC Stress Effect on LDO PSRR

A combination of AC and DC stress is a much more realistic form of transistor aging. AC stress is applied on Chip 3 and Chip 4 to observe the effect of HCI on the PSRR of the LDOs along with DC stress. During this time, the exact setup of the DC stress is maintained except, the load current of the LDO is varied from 0.9mA-1.1mA. Also the reference voltage of the EA is varied from 500mV to 700mV. After 4 hours of accelerated HCI and BTI aging, both the temperature (using thermostream) and V_{DD} are brought back to nominal values.

The aged PSRR is shown in Figure 7. The change in the DC value of PSRR (2-5dB) is much more compared to the degradation (1.6dB) due to only the DC stress (see Figure 4). The marked difference between the aged and the fresh LDO PSRR is due to the shift in the position of the poles. The pole (ω_1) shifts from 1.7MHz in the fresh chip to 800KHz for the aged chips immediately after cooling to 25°C. Due to aging of the LDO, non-dominant pole (ω_2) which was not visible before 250MHz for the fresh LDOs shifts and appears

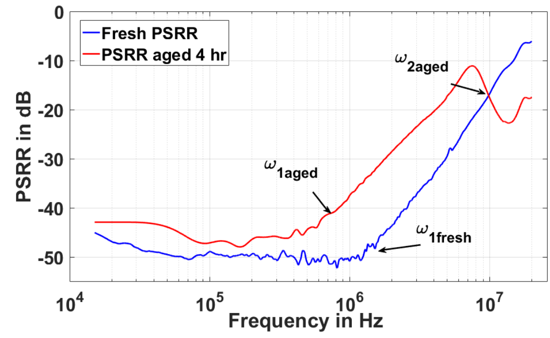

Fig. 7: Silicon results showing PSRR aging degradation owing to AC stress at 105°C using thermostream for 4hrs with 10% increase in V_{DD}. Data recorded after cooling the chip to 25°C with thermostream.

around 10 MHz for the aged LDO. Thus owing to shifting of the above poles to much lower frequency compared to the fresh LDOs, the PSRR curves completely transform in region 2 with the combined effect of DC and AC stresses.

Shift of ω_1: In the silicon measurements (refer to both Figure 4 and 7, the dominant pole defined previously (ω_o) at the output of LDO appears around 30-50KHz. For low load currents (1mA) in our case, the output impedance of the PT is high. The LDO's output appears to be an ideal current source due to the negative feedback of the control loop. The pole formed by the output capacitor and the pass element occurs at a relatively low frequency (30-50KHz) in Figure 7, so PSRR tends to increase at low frequencies. The high dc gain of the output stage at low currents also tends to increase the PSRR at frequencies well below the unity-gain point of the error amplifier. The pole (ω_1) seen at 1-2 MHz for the fresh IC shifts to a lower frequency of 800 KHz after AC stress. This can be attributed to reduction in the unity gain bandwidth of the LDO due to AC electrical stress. The V_{REF} and the load current were continuously fluctuated during the AC stress due to which HCI affected both the input transistors of the EA and the PT causing marked changed in the gain bandwidth of the regulator which shifted from 1.7 MHz to 800 KHz.

Shift of the ω_2: A new pole appeared at higher frequency of $\approx$ 10 MHz which was not present previously for fresh ICs. This can be due to the degradation of the gate capacitance and equivalent resistance at gate of the PT. For a generic LDO (refer: Figure 1), the degradation of I_{D} with transistor aging increases small signal output resistance (r_{ea} in Eqn (4)), thus shifts the pole to a lower frequency. Along with the resistance, the gate and drain capacitance of the PT may also increase with the temperature and voltage stress, thus shifting ω_2 to a lower frequency in aged ICs compared to the fresh ones.

Shift of PT capacitances: To observe the shift in drain and gate capacitances, we applied an AC signal at the source of the PT. The amplitude of the signal is low such that the LDO is in off state. We applied a 34KHz sine signal at the source with an amplitude of 50mV (100mVp-p). Then, we recorded the AC signals obtained at the gate and drain terminals of the PT. There was a shift in phase and amplitude in the signals collected at the gate and drain terminals compared to that given to the source terminal. The AC signal at the gate is very low in amplitude (approximately 1-2mAp-p). This can

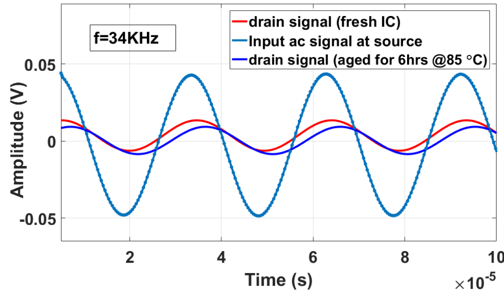

Fig. 8: Phase shift in the AC signal recorded from the drain terminal of the PT after 6 hour of DC stress. The phase shift implies a change in the impedance between the drain and source.

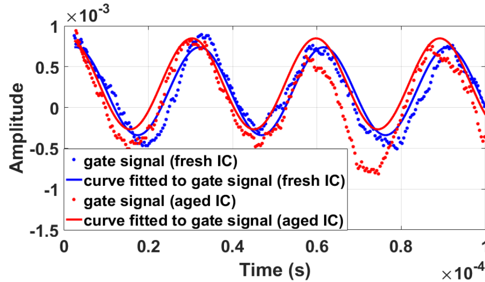

Fig. 9: Phase shift in the AC signal recorded from the gate terminal of the PT after 6 hour of DC stress. The phase shift implies a change in the impedance between the gate and source.

be because of the fact that the probe capacitance forms a path to ground which pulls down the gate signal amplitude. The signal obtained from the drain is also low (approximately 20mAp-p) as the LDO including the PT is not in operating condition. Since the LDO is not operating, this shift is due to the collective impedance in between the source, gate and drain terminals. After initial data recording, the LDO dies were again subjected to DC stress as mentioned above. After the aging process, the phase shift between the AC signals at the drain and source terminals as well as the gate and source terminals changed as shown in Figures 8 and 9. The change in the phase angle is evidence of the change in total impedance between the gate-source and source-drain which can explain the shift of poles previously seen in Figure 7.

Referring to the equivalent circuit of the gate and drain capacitances of the PT as shown in Figure 10, the path from source to drain can be modelled as an equivalent series resistor capacitor circuit. As the LDO is powered off, R_{dsoff} is very large, thus we have considered it as an open circuit. v_{a1} is the amplitude of the ac signal given at source and v_{a2} is that collected at drain. The phase-shift is given by: $\theta = \tan^{-1}\frac{X_c}{R}$ The initial phase shift before aging is $\approx 30^\circ$ while after aging it reduces to $\approx 25^\circ$. With a rough estimation using equation above it can be calculated that the equivalent capacitances increases by $\approx 23\%$ considering the output equivalent resistance is constant.

V. Conclusion and Future Work

In this paper, we have analyzed the PSRR degradation of an LDO with respect to NBTI and HCI electrical stress (an emulation of natural transistor aging). With recycling, ICs/SoCs undergo natural transistor aging, thus the aging model of the PSRR degradation can detect recycled LDOs. As LDOs are universal in any IC/SoC, this can be a one

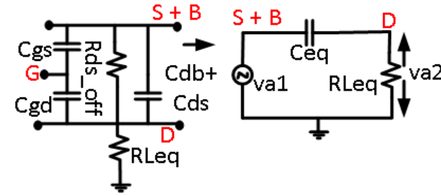

Fig. 10: Equivalent circuit showing the gate and drain capacitances of the PT.

size fits all solution for detection of any recycled IC/SoC. Our experimental results show substantial degradation of the LDO PSRR with respect to DC (1.6dB of DC PSRR) as well as AC stress (shifting of poles to lower frequency). This degradation has been explained by characterizing the aging degradation of the intrinsic electrical properties of the pass transistor of the LDO. Our experiments also provide evidence of substantial degradation of PT and it's parasitics with aging. In future, we plan to extend our experimental results to formulate a concrete aging model for the LDO PSRR, which can be utilized with machine learning algorithms to improve detection of recycled ICs.

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