# Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs)

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***Abstract*—Physically Unclonable Functions (PUFs) were introduced over a decade ago for a variety of security applications. Silicon PUFs exploit uncontrollable random variations from manufacturing to generate unique and random signatures/responses. Existing research on PUFs has focused on either PUF design at the architectural level or optimization of lithography to increase sensitivity to random process variations. however, such sources of randomness may become limited during standard CMOS manufacturing as processes continue to mature especially with the advances in design for manufacturability. In this paper, poly-Si is proposed to improve PUF quality at the materials level. Compared to conventional single crystal Si (sc-Si), defects and trapped charges resulting from the random distribution of crystal grains and grain boundaries (GBs) in poly-Si offer considerable random variations. By using poly-Si only in the PUF region in devices, the randomness of the PUF can be enhanced without impacting other functional circuits and thus the IC yield can be maintained. RO-PUF simulation results based on a poly-Si field-effect-transistor (FET) model show that compared to sc-Si based PUFs, the reliability of poly-Si based PUFS can be improved from 89.18% to 98.82%.**

## I. Introduction

With increasing demands on security, physical unclonable functions (PUFs) have been introduced to provide promising solutions to many security applications, such as identification, authentication, and secret key storage. Silicon PUFs can be easily embedded in electrical devices and generate unique challenge-response-pairs (CRPs). The performance of PUFs can be evaluated by the quality of CRPs, using metrics such as uniqueness, unpredictability and reliability. The uniqueness requires each PUF to generate a distinct signature from other PUFs. The unpredictability requires the generation of response to any challenge be impossible to model. The reliability requires stable correspondence between challenges and responses.

For better PUF quality, a significant random variation is desired. The challenge is that such variation is typically detrimental to other parts of the chip and can result in yield loss. Extensive research has been devoted to develop novel PUF designs in order to improve PUF performance while maintaining the process yield [1]–[3]. However, improving the source of randomness (lithography) has not been investigated as mush. The overhead could also be considerable with those novel designs. Research targeting lithography to increase the variation has also been reported in [4], [5]. A novel optical proximity correction (OPC) method was proposed to increase the device geometry variations within PUF circuit region while allowing conventional OPC to suppress geometry variations in other parts of the circuit.

In this paper, we propose a more effective approach for improving randomness at device materials level by employing poly-Si as substrate material for transistors used in PUF. The randomness in poly-Si is from the random distribution of crystal grains and grain boundaries (GBs), which are formed during the materials growth. Unlike the OPC methods that only affect device geometry size, the randomness introduced by the grains and GBs influences the randomness of transistor threshold voltage and effective mobility. In addition, the fabrication of poly-Si devices is compatible to CMOS processing and can be performed selectively in regions associated with the PUF. We summarize our major contributions as follows:

- Poly-Si is introduced for PUFs to increase the random variations. We highlight the compatibility of such an approach to conventional CMOS processing
- A quantitative trapping that describes the electrical properties of poly-Si is combined with short-channel transistor model to simulate the poly-Si PUFs performance.
- Simulation results on a ring-oscillator PUF design reveal that compared to conventional single crystal Si PUFs, poly-Si PUFs present improved reliability and randomness.

The rest of this paper is organized as follows. In Section II, we provide background on silicon PUFs, transistor performance and poly-Si. In Section III, we present the design of PUF devices based on poly-Si and discuss the important parameters of material and device for poly-Si PUFs. In Section IV, models at different levels, from material level to device level and eventually to circuit level, are built for the simulation of poly-Si PUFs performance. Results are discussed in Section V and finally, the conclusion is given in Section VI.

## II. Preliminary

### A. Silicon PUFs

Most silicon PUFs can be categorized into two basic classes: delay-based PUFs and memory-based PUFs. The former ones, such as arbiter PUF and ring oscillator PUF (RO-PUF), exploit the random variations in timing of a set of symmetric circuit

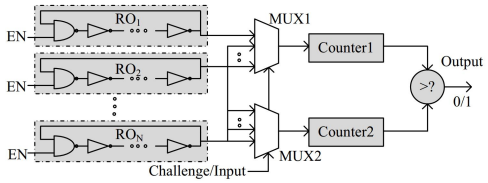


Fig. 1. Ring oscillator PUF.

paths, while the latter ones, such as SRAM PUF and butterfly PUF, exploit the random settling behavior of bistable circuit elements. Although the approaches proposed in this paper are generic, we take the RO PUF as a running example for simplicity.

### B. RO-PUF

RO-PUF is a widely discussed architecture that does not need rigorous design and can be implemented in ASIC or reconfigurable platforms [6]. The schematic of a typical RO-PUF is shown in Fig. 1. It has $N$ identical ring oscillators (ROs), two multiplexers, two counters and one comparator. Each of the ROs run with slightly different frequencies due to manufacturing process variation. A challenge is applied to both MUXes so that one pair of ROs is selected in order to extract the frequency difference within the pair and generate a 1-bit response. The number of oscillations of each of the RO-pairs is counted for a fixed time interval (known as comparison time) using the counters. The outputs of the counters are then compared using the comparator, and the comparator result is set to '0' or '1' based on which oscillator from the selected RO pair is faster.

### C. Transistor

The propagation delays of transistors play an important role in delay-based PUF. The delays are defined by $t_{PHL}$ and $t_{PLH}$, which are the 50% propagation delays for signal high-to-low and low-to-high respectively and given by:

$$t_{PHL} = \frac{\alpha_n C}{\mu_n C_{ox}(W/L)_n V_{DD}} \tag{1}$$

$$t_{PLH} = \frac{\alpha_p C}{\mu_p C_{ox}(W/L)_p V_{DD}} \tag{2}$$

where subscripts $n$ or $p$ indicate an n-type or p-type transistor, $C$ is the effective load capacitance for the given stage, $W/L$ is sizing ratio, $\mu$ is mobility, $C_{ox}$ is effective gate capacitance, $V_{DD}$ is supply power, and $\alpha$ is given by:

$$\alpha = 2 \Big/ \left[\frac{7}{4} - \frac{3V_t}{V_{DD}} + \left(\frac{V_t}{V_{DD}}\right)^2\right] \tag{3}$$

where $V_t$ represents threshold voltage [7]. Randomness from the manufacturing processes results in slightly varied $W$, $L$, $\mu$, $C_{ox}$ and $V_t$, which are exploited for PUFs. Meanwhile, as indicated by Eqn. (1) to (3), the variation of $V_{DD}$ can also vary the delay time. Since the $V_{DD}$ is mainly affected by environmental factors, such variation can make the PUF device give different response even upon the same challenge, which makes the PUF less reliable. To improve the performance and reliability of PUFs, large variations from $W$, $L$, $\mu$, $C_{ox}$ and $V_t$ are desired.

### D. Poly-Si

Poly-Si is polycrystalline form of silicon. Extensive studies have been done on poly-Si since one century ago and now it is widely used in many devices, such as solar cells and thin film transistors [8], [9]. Compared to single crystal silicon (sc-Si) that can be considered as an infinite crystal grain, poly-Si consists of many small single crystal grains with randomly distributed orientation and grain boundaries (GBs). The GBs introduce structure defects (*e.g.* dislocation) in crystal Si, and trap charges and/or impurities, which dramatically affect the electrical characteristics of Si. Although in most cases such effects are considered as degradation for electrical devices, it is valuable for PUFs as the material properties are highly localized and thus result in significant variations. In fact, poly-Si has already been studied for hardware security even before the PUF concept was proposed. An artificial fingerprint device module was reported in [10]. Variations in the subthreshold current of poly-Si based thin film transistors (TFTs) was used to generate the unique digital ID. Poly-Si thin film can be prepared via different deposition techniques, including sputtering, low-pressure chemical vapor deposition (LPCVD) and plasma-enhanced chemical vapor deposition (PECVD). With different preparation methods and post-annealing conditions, the properties of poly-Si can vary in a wide range. For example, the average grain size from a few nanometers to a few micrometers can be obtained and defect density on GBs has been reported as $10^{12}$/cm$^2$ to $10^{14}$/cm$^2$ [11].

## III. Poly-Si PUF Design

As discussed in the previous section, poly-Si with random distributed GBs is promising to serve as a variation source for PUF devices. The fabrication of PUF based on poly-Si will include material preparation, transistor fabrication and circuit realization, which are discussed below.

### A. Poly-Si deposition

Crystal silicon wafer is used here as the substrate. The PUF regions are first etched into substrate for certain depth (*e.g.* 200 nm) by dry etching, then isolation layer and poly-Si are successively deposited into the etched PUF regions, making the wafer surface becomes planar again (for the convenience of the subsequent processing). After the deposition, annealing is performed to modify the properties of poly-Si, such as grain size and defect density.

### B. Transistor fabrication

Most TFTs including poly-Si based ones can be fabricated with conventional CMOS processing, which has been thoroughly discussed in prior work [10]. The difference between typical TFTs and the poly-Si transistors discussed in this paper is that the former ones are usually fabricated on non-silicon wafer substrate for cost control while the later ones are

fabricated on the same wafer together with other functional circuits.

### C. PUF structure

ROs consist of an odd number of inverters, typically containing one n- and p-type transistor each. For simulation purpose, we have generated responses from 100 RO-PUFs using both crystalline and polysilicon transistors. Each of the ring oscillators has 21 inverter stages, and each PUF has 256 ROs to produce 128 possible CRPs. Considering the typical feature size of common devices on the market and the calculation complexity, 90 nm node is used in this study [12].

## IV. Modeling

The model built for simulation is divided into 3 steps: (1) generation of poly-Si structure, (2) calculation of transistor parameters, and (3) the simulation of ROs. As this model is being developed to verify the potential benefits of poly-Si PUFs rather than to accurately predict the device performance, several simplifying assumptions are made, as mentioned in following discussion.

### A. Poly-Si structure

Carrier trapping model [13] is employed to describe the properties of poly-Si in this paper. For simplification, we assume the material properties inside crystal grain are the same as bulk sc-Si. In addition, we assume that the charges trapped on GBs are fixed and we only consider the influence of trapped charges as the difference between poly-Si and sc-Si. The distribution of crystal grains in poly-Si is generated via Voronoi diagram. As the initial forming of each crystal grain in poly-Si starts from the uniformly distributed surface nucleation, the coordinates of Voronoi seed points are first randomly generated following uniform distribution within the PUF region. Then the Voronoi edges (*i.e.* grain boundaries) are generated accordingly, as shown in Fig. 2 (average grain size 300 nm×300 nm). For convenience, we assume the GBs are parallel to each other in the depth direction and perpendicular to the substrate surface. The thickness of GBs is neglected and the density of trapped charges ($N_{GB}$, in unit of /cm$^2$) on GBs is assumed to be uniform. The doping concentration ($N_G$, in unit of /cm$^3$) and effective carrier density in crystal grains are assumed to be equal and uniform.

### B. Transistor parameters

Since PUFs leverage inherent manufacturing process variations to generate unique responses, we have incorporated systematic and random variations with spatial correlations [14], [15] with a $3\sigma$ deviation in inter-die and intra-die process equal to 10% and 5% of mean values respectively. Table I shows the physical parameters and respective mean values used in the simulations. For poly-Si devices, the transistors are located on as-generated poly-Si surface, with rectangle channel regions shown in Fig. 2. For single crystal devices, the transistor arrangement is the same as poly-Si ones but on sc-Si substrate without grains or grain boundaries. Individual transistor parameters including threshold voltage, effective mobility and capacitance are considered. A power supply ($V_{DD}$) variation with a $3\sigma$ deviation of 8% is also incorporated to analyze the robustness of the system for 20 trials.

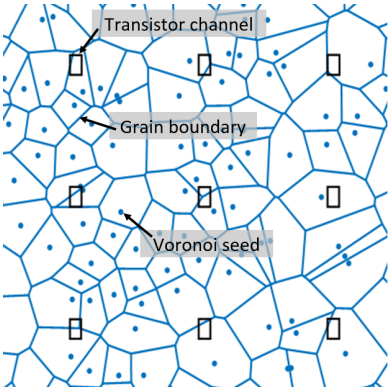

Fig. 2. The channels of the transistors on poly-Si.

TABLE I
Simulation Parameters

| Parameters | Mean Value |
|---|---|
| Channel Length ($L$) | $90nm$ |
| NMOS Channel Width ($W_n$) | $120nm$ |
| PMOS Channel Width ($W_p$) | $240nm$ |
| NMOS Oxide Thickness ($T_{ox,n}$) | $2.05nm$ |
| PMOS Oxide Thickness ($T_{ox,p}$) | $2.15nm$ |
| Power Supply ($V_{DD}$) | $1.1V$ |

*Threshold voltage ($V_t$).* The approach we use to determine $V_t$ is based on the evaluation of surface potential in the channel [16]. According to superposition principle, the surface potential $\Psi(x, y)$ can be described as:

$$\Psi(x, y) = U(x, y, z)|_{z=0} + \Phi(x, y, z)|_{z=0} \tag{4}$$

where $x$, $y$ and $z$ (0 for surface) are along the direction of channel length, channel width, and substrate thickness, respectively; $U$ is the analytic solution of the electrostatic potential that satisfies the boundary conditions at gate, source and drain; and $\Phi$ is the potential contributed by trapped charges on GBs and the corresponding mirror charges in gate. The details of calculation and more equations can be found in [16] and [17].

*Effective mobility ($\mu$).* The effective mobility ($\mu$) is defined as:

$$\mu = \frac{L}{W} \cdot \frac{-qN_cI_d}{V_{ds}} \tag{5}$$

where $q$ is the charge of one carrier, $N_c$ is the carrier density in inverted channel, $I_d$ is current from source to drain, $V_{ds}$ is the voltage applied over source and drain. To obtain $I_d$, we assume the current passes through the channel in parallel flows for simplicity (the same assumption is also used for $V_t$ calculation [16]). The channel is divided into parallel "lanes". Current passing through each lane is calculated based on the local $V_t$ of each lane obtained during the $V_t$ calculation, via ballistic model [18]. The sum of current from all the lanes in the channel gives the value of $I_D$. In a real device, because of the carrier scattering on GBs, the mobility will be significantly

lower. Since the physical details is complicated and has not yet been completely understood, it is difficult to include the scattering effect in our model. Meanwhile, although numerical approaches for scattering effect calculation has been proposed [19], they are for the property of bulk poly-Si and thus not appropriate for this study. To collect more accurate effective mobility data, we plan on characterizing real device in future work. Nevertheless, the variation from poly-Si that is discussed in this paper generally makes the transistors slower (larger delay) than sc-Si transistors. The scattering on GBs will further increase the delay by lowering the effective mobility in channels. Therefore, the scattering effect should give more variations and thus not contradict the advantages of using poly-Si for PUFs.

*Capacitance*. As we assume the trapped charges on GBs are fixed and not affected by applied voltage, they do not contribute to capacitance, which means the capacitance of poly-Si devices (such as gate-to-drain capacitance, drain-to-source capacitance, *etc.*) is considered as the same to sc-Si devices. Of course, the situation in real device is much more complicated and further investigation is necessary for an accurate predictive model.

### C. Ring oscillators

For an ideal ring oscillator, the frequency produced is given by:

$$f_{0,ideal} = \frac{1}{2Mt_P} \tag{6}$$

where, $M$ is the number of stages (inverters) in the given RO, and $t_p$ is the propagation delay through the inverter.

However, this ideal case does not hold for RO-PUFs. Since each of the ROs, including the individual transistors in them, experience manufacturing process variations, the frequencies of the ROs slightly differ from each other even though they are identically designed in the RO-PUF. Thus the frequency of an RO, incorporating manufacturing variation, is given by:

$$f_0 = \frac{1}{2\sum_{i=1}^{M} t_{P,i}}; i = 1, 2, ..., M \tag{7}$$

where, $t_{P,i}$ denotes the propagation delay of stage $i$:

$$t_{P,i} = \frac{1}{2}(t_{PHL,i} + t_{PLH,i}); i = 1, 2, ..., M \tag{8}$$

Note that $t_{PHL,i}$ and $t_{PLH,i}$ are random variables that can be calculated by Eqn. (1) and (2).

## V. Results and Discussion

### A. Influence of Poly-Si on Transistors

*Density of trapped charges.* We first study the influence of $N_{GB}$ on the poly-Si based transistors. According to reported $N_{GB}$ range [11], $2\times10^{12}$/cm$^2$, $10^{13}$/cm$^2$, and $5\times$ $10^{13}$/cm$^2$ are chosen for the simulation. With two grain boundaries (Fig. 3a), the surface potential in the n-type channel under bias ($V_g = 0$, $V_{ds} = 1.1$ V) is calculated. The resulting surface energy distribution (for electrons) is shown in Fig. 3b-d. As revealed, when $N_{GB}$ is low ($2\times10^{12}$/cm$^2$), the surface energy barrier resulting from the grain boundary is insignificant (Fig. 3b), which gives $V_t$ of 0.33 V (close to the $V_t$ of sc-Si transistor, 0.31 V). When $N_{GB}$ is higher ($1\times10^{13}$/cm$^2$), the surface energy barrier height increases (Fig. 3c), resulting in higher $V_t$ of 0.44 V. Further increasing $N_{GB}$ to $5\times10^{13}$/cm$^2$, the height of energy barrier is over 1 eV and $V_t$ is 0.99 V (Fig. 3d). Practically, $N_{GB}$ is mainly determined by the defect density on GBs and temperature. Since the defects are formed during the poly-Si thin film preparation, proper preparation methods is particularly important to obtain poly-Si device working under designed working voltage. Post-annealing is also important as the micro structure of poly-Si can be modified by annealing, which changes the distribution of the defects in poly-Si. About the temperature effect, researchers reported the I-V feature of poly-Si transistors in [10], claiming that although the effective mobility in transistor increased with temperature, stable and precise recognition could be still obtained by comparing the characteristics of plural transistors. The methodology employed in that paper is very similar to the mechanism of response generation in delay-based PUFs.

*Grain size.* The second important parameter of poly-Si is the average grain size ($L_G$). To evaluate the influence, different $L_G$ values from 1 nm to 3 $\mu$m are used for the calculation of $V_t$ and $\mu$. The sample size is 100 for each set. Geometry variations in channel length, channel width, channel doping density and gate oxide layer thickness are also included, assumed to follow a normal distribution with $3\sigma$ equals 5% of the mean value.

TABLE II
Grain Size Vs. Variation

| Grain Size | 100 nm | 300 nm | 1 µm | 3 µm | sc-Si |
|---|---|---|---|---|---|
| Channels w. GB | 100/100 | 66/100 | 17/100 | 4/100 | 0/100 |
| Max Vth (V) | 0.481 | 0.479 | 0.368 | 0.347 | 0.324 |
| Min Vth (V) | 0.302 | 0.296 | 0.294 | 0.286 | 0.282 |
| Mean Vth (V) | 0.376 | 0.340 | 0.313 | 0.309 | 0.306 |
| Dev. (Std/Mean) | 9.96% | 11.9% | 5.14% | 3.22% | 2.67% |

The statistic results are listed in Table II. "Channels w. GB" means the number of transistors with channel region containing at least one grain boundary out of the total 100 transistors. With increasing grain size, the density of GBs decreases and the number of channels containing GBs decreases consequently. Decreasing GB density can also explain the maximum, minimum and mean $V_t$: higher GB density results in higher trapped charge density, thus higher surface energy barrier and higher $V_t$. To consider the variations of $V_t$ on device with different grain sizes, there are two extreme situations. One is when the grain size is scaled down to sub-nanometer, which is just like amorphous silicon. The other is when the grain size is so large that few boundary can be found in channels, which makes the transistors like sc-

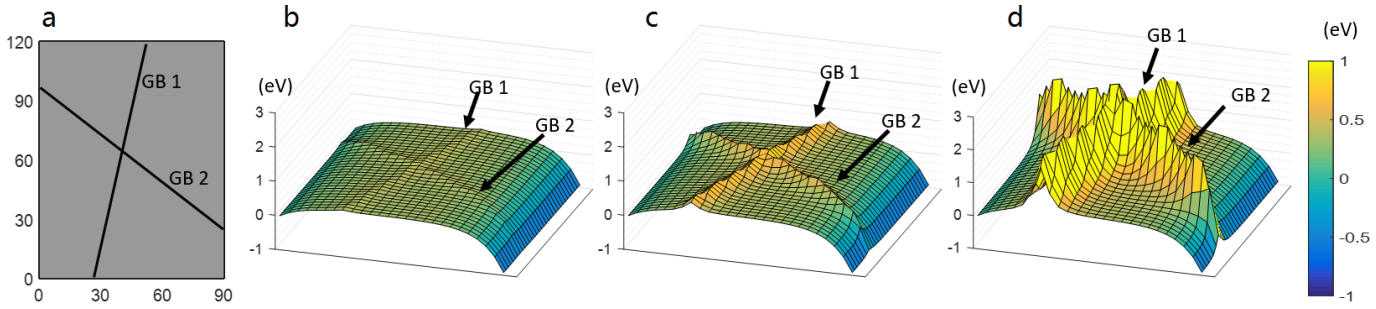


Fig. 3. Surface potential.

Si ones. For both situations, the randomness decreases as the material properties are more uniform. To enhance the variation, the grain size should be properly controlled. As revealed in Table II, the $V_t$ variation decreases quickly when the grain size becomes larger than 1 µm. When the grain size becomes smaller than 300 nm, the variation decreases too, although more slowly. Considering both the mean value and the standard deviation of $V_t$, 300 nm is the optimized for 90 nm devices for PUF application.

### B. Security Analysis

In this study, we used uniqueness, reliability, and uniformity to measure PUF quality as described in [20]. As dicussed in Section III-C, there are 256 ROs in each PUF, paired into 128 pairs. By comparing the RO frequencies, a 128-bit response is obtained from each PUF. To incorporate spatially correlated systematic variations, 5 levels of quad-tree partitioning [14] are performed for each PUF, dividing the device into 16 grids at bottom level with each grid containing 16 ROs. Two pairing strategies are used to generate the PUF responses: 1) pairing spatially adjacent ROs (adjacent pairing, *e.g.* RO1 and RO2) and 2) pairing spatially apart ROs (apart pairing, *e.g.* RO1 and RO129). The resulting bits are given by:

$$r_{adj,i} = \begin{cases} 0, & \text{if } f_{2i-1} > f_{2i}, \\ 1, & \text{else.} \end{cases} \qquad i = 1, 2, ...128 \tag{9}$$

$$r_{adj,i} = \begin{cases} 0, & \text{if } f_{i} > f_{i+128}, \\ 1, & \text{else.} \end{cases} \qquad i = 1, 2, ...128 \tag{10}$$

where $r_{adj,i}$ and $r_{apt,i}$ are the $i$th bit generated by adjacent pairing and apart pairing, respectively; $f_i$ is the frequency of the $i$th RO. With such setting, 20 trials with varied $V_{DD}$ ($3\sigma = 2\%$) are performed on both poly-Si PUFs and sc-Si PUFs, via both adjacent pairing and apart pairing.

The PUFs test results are listed in Table III, and the inter-HD and intra-HD are plotted in Fig. 4. By adjacent pairing, the uniquenesses of both sc-Si and poly-Si PUFs are satisfying (0.4941 for poly-Si and 0.4989 for sc-Si). The sc-Si PUFs reliability is poorer (0.8930) compared to the poly-Si ones (0.9886). This can be explained by a lack of significant device variation on sc-Si PUFs. By adjacent pairing, the device variation for sc-Si PUFs is only from lithography, which is typically small between adjacent two ROs [21]. Even a small $V_{DD}$ variation is therefore possible to flip the output bit. For poly-Si, extra device variation contributed by randomly distributed GBs makes the PUFs much more reliable. The uniformities of both sc-Si and poly-Si PUFs are around 0.5, with small standard deviations.

TABLE III
TEST RESULTS

| | sc-Adj | poly-Adj | sc-Apt | poly-Apt | ideal |
|---|---|---|---|---|---|
| Uniqueness Mean | 0.4989 | 0.4941 | 0.5076 | 0.5019 | 0.5 |
| Uniqueness Std | 0.0416 | 0.0414 | 0.2088 | 0.1194 | 0 |
| Reliability Mean | 0.8930 | 0.9886 | 0.9813 | 0.9850 | 1 |
| Reliability Std. | 0.0036 | 0.0013 | 0.0034 | 0.0020 | 0 |
| Uniformity Mean | 0.5076 | 0.4878 | 0.4714 | 0.4893 | 1 |
| Uniformity Std. | 0.0434 | 0.0427 | 0.1859 | 0.1551 | 0 |

By apart pairing, systematic device variation from lithography, which is spatially correlated, is introduced. As shown in Table III, the uniqueness mean values of sc-Si and poly-Si PUFs are still around 0.5, but the uniqueness standard deviations increase from 0.0416 and 0.0414 to 0.2088 and 0.1194, respectively. This can be explained by the biases from the systematic deviation. Such biases are between paired sets of ROs (*e.g.* RO1∼RO128 vs. RO129∼RO256), which makes the average delay of the first set of ROs is either less or larger than the second set. Therefore, the RO comparing results can be biased, affecting the uniqueness of PUF outputs. As the chances are even for the first RO set to be faster or slower than the second one, the mean value of uniqueness obtained from all of 100 PUFs are still around 0.5. However, the much larger standard deviations compared to the adjacent pairing indicate a considerable amount of PUFs are biased, thus more inter-HDs move towards either '0' or '1', as shown in Fig. 4 c and d. Comparing poly-Si devices to sc-Si ones, it can be noticed that the standard deviation is controlled better on poly-Si ones (0.1194 vs. 0.2088), as the additional randomness from the GBs balances the non-random systematic deviation.

As for the reliability, because of the considerable systematic device variation introduced, the PUFs outputs become more

robust to $V_{DD}$ deviation and the reliability of sc-Si PUFs is significantly improved compared to the adjacent pairing (from 0.8930 to 0.9813). For poly-Si, as the additional systematic variation is insignificant compared to the random variation from GBs, it does not make the PUFs more reliable. Instead, the larger $V_{DD}$ variation compared to the adjacent pairing decreases the reliability of poly-Si PUFs slightly (from 0.9886 to 0.9850). The uniformities of sc-Si and poly-Si PUFs are around 0.5, with larger standard deviation compared to the adjacent paring, as shown in Table III. The explanation of the uniqueness applies to the uniformity too: even chances for the first sets of ROs to be faster or slower than the second sets make the mean value obtained from all 100 PUFs around 0.5 while biased comparing in each pair of RO sets results in a large standard deviation. Again, randomness from the GBs in poly-Si devices helps to balance the bias and gives a better control on the standard deviation.

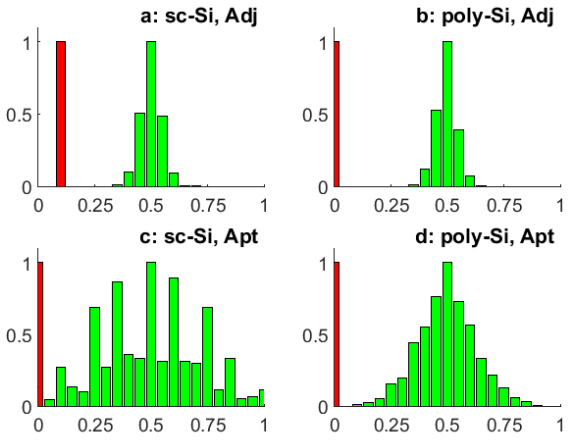


Fig. 4. Normalized histogram of uniqueness and reliability obtained from poly-/sc-Si PUFs via adjacent/apart pairing (green bars for uniqueness and red bars for reliability).

By comparing adjacent and apart pairings, we find that the adjacent pairing should be used to avoid systematic deviation, which helps to improve the uniqueness and uniformity of PUF devices. The conclusion is consistent with the result reported in [22]. The challenge on reliability mentioned in [21] can be overcome by using poly-Si, which introduces an enhancement of randomness at the material level.

## VI. Conclusion

In this study, we introduce poly-Si for PUF devices to bring in selective enhancement of randomness from materials. As independent from device patterning processing, the enhancement of such randomness will not compromise the accuracy of OPC and thus the loss of yield can be avoided. Simulation results clearly show that the uniqueness of poly-Si PUFs is as good as that of sc-Si ones, while the reliability and uniformity of poly-Si PUFs are improved. In future work, we plan on fabricating poly-Si RO PUFs, studying the properties at different temperatures and comparing the experimental results with the simulation results.

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