Non-destructive PCB Reverse Engineering Using X-ray Micro Computed Tomography

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Abstract

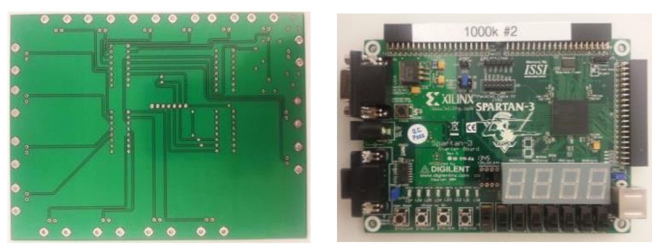
Reverse engineering of electronics systems is performed for various reasons ranging from honest ones such as failure analysis, fault isolation, trustworthiness verification, obsolescence management, etc. to dishonest ones such as cloning, counterfeiting, identification of vulnerabilities, development of attacks, etc. Regardless of the goal, it is imperative that the research community understands the requirements, complexities, and limitations of reverse engineering. Until recently, the reverse engineering was considered as destructive, time consuming, and prohibitively expensive, thereby restricting its application to a few remote cases. However, the advents of advanced characterization and imaging tools and software have counteracted this point of view. In this paper, we show how X-ray micro-tomography imaging can be combined with advanced 3D image processing and analysis to facilitate the automation of reverse engineering, and thereby lowering the associated time and cost. In this paper, we demonstrate our proposed process on two different printed circuit boards (PCBs). The first PCB is a four-layer custom designed board while the latter is a more complex commercial system. Lessons learned from this effort can be used to both develop advanced countermeasures and establish a more efficient workflow for instances where reverse engineering is deemed necessary.

Keywords: Printed circuit boards, non-destructive imaging, X-ray tomography, reverse engineering.

Introduction

Reverse engineering is a process where the goal is to reproduce, duplicate, or enhance chips and systems based on the study of an original object/system. For electronic systems, reverse engineering (RE) could be performed at chip, board, and system levels. Since such electronics typically consist of multiple layers, reverse engineering involves obtaining the internal structure and connections of all layers through either a destructive process of delayering or non-destructive processes. In a destructive process, delayering is followed with imaging of every layer before the next round of material removal. On the other hand, a non-destructive process consists of imaging tomography, which can be used to image the whole system or board without delayering. In either case, the analysis can be automated or manual and ultimately results in a netlist [1] that can be used to reproduce the system.

Reverse engineering can be performed by groups with "honest" intentions or "dishonest" intentions. "Honest" intentions include verification of a design for the purposes of quality control, fault and failure analysis, analysis of the features of a competitor's product, counterfeit detection, Trojan detection, confirmation of intellectual property, approved redesign of an obsolete product, and education [2][16][17]. In many countries, reverse engineering is even legal as long as patents and design copyrights are not violated [3]. When reverse engineering is performed with the intention of performing cloning, piracy, Trojan insertion, or counterfeiting, the intention is "dishonest". If RE results in a working copy of the system, it is called a cloning attempt [4]. "Dishonest" parties could sell large amounts of cloned or counterfeit products without incurring the same development costs as the IP owner [5]. Beyond cloning, RE of electronic systems could also become a major motivation for Trojan insertion. Since a dishonest party is cloning an electronic system, he/she will have the capability of adding malicious circuitries or firmware to the system as well.



(a) (b)

Figure 1: (a) Four layer custom board, (b) Commercial Xilinx Spartan-6 starter board.

In this paper, we focus on board-level reverse engineering since a printed circuit board (PCB) is the fundamental component of any electronic system. A PCB is a laminated non-conductive material that connects electronic components via conductive copper traces. Electronic components and chips are mounted on the board and are electrically interconnected with these traces. The board might be single or multi- layered depending on the complexity of the system. A RE team could analyze the outer layers of an authentic board to find the components mounted on it, its traces, and its ports. After that, they could delayer the multi-layered board to reveal the connectivity, traces, and vias within its internal layers.

We use a Zeiss Versa 510 X-ray machine to demonstrate how easy it is today to perform RE on PCBs with suitable equipment and expertise. Our process is both fast (4.23

scan/hour) and partially non-destructive. Although we might need to remove the components from the board to reduce the noise level in the images, comparing with traditional destructive methods where serial sectioning had to be done, this method can be considered as one that is faster and easily repeatable. In other words, it is more amenable to automation from start to finish. We illustrate our technique on a small custom PCB first (see Fig. 1 (a)) as a proof of concept. Next, the same scanning process is applied to a 6 layer commercial Xilinx Spartan-6 starter board as shown in Fig. 1(b). The entire process consists of optimizing parameters for X-ray, performing X-ray imaging, and performing image processing. These steps are discussed in detail along with the results and potential countermeasures in the remainder of the paper.

X-ray Imaging

Tomography is a non-invasive imaging technique that makes it possible to visualize the internal structure of an object without interference of over- and under-layer structures. In this paper, micro X-ray computed tomography is performed using the Zeiss Versa 510, which has a maximum power of 160 KV for its source, to acquire the structural information of different PCBs. X-ray tomography gives us the opportunity to extract the geometrical information of traces, via holes and connections on PCB layers. Note that all PCB layers (front, back, and internal) be captured in a *single imaging session.*

Optimizing Image Acquisition Parameters

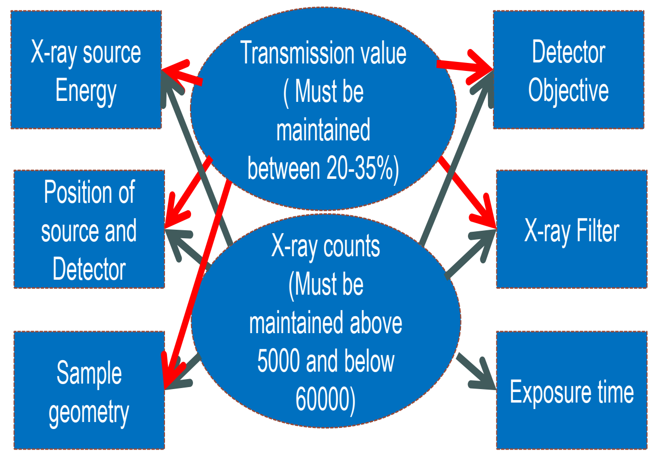
The principle of tomography is to acquire a stack of two dimensional (2D) images and then use mathematical algorithms such as direct Fourier transform and center slice theory [6] to reconstruct the three dimensional (3D) image. These 2D projections are collected from many different angles depending on the quality needed for the final image. The object properties, such as its dimension and material density, are important to consider in selection of the tomography process parameters which include:

- *Source power*: correlated to the X-ray energy and amount of penetration
- *Detector objective*: determines the field of view and resolution range
- *Filtering*: controls the dose which allows higher energy X-rays to penetrate
- *Distance of source and detector from sample*: inversely proportional to number of counts
- *Number of X-ray projections*: identifies the angular increment for each rotation for sample during tomography
- *Exposure Time*: linearly related to counts and determines the total time and, consequently, the cost of scanning.

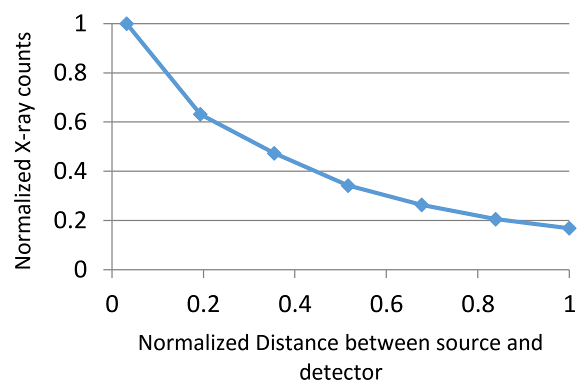
These parameters can affect the pixel size and signal-to-noise ratio, which must be optimized based on the region-of-interest. Internal and external structure can be analyzed when the 3D image is reconstructed, which needs center shift and beam hardening tuning. [7].

Trade-off between Pixel Size and X-ray Counts

The most critical parameter for defining the quality of 3D reconstructed images is the pixel size. Based on it, many other parameters such as distance of source and detector from the sample (geometric magnification) and detector objective (similar to optical magnification) will be tuned.



(a)



(b)

Figure 2: a) Effecting parameters on X-ray imaging b) X-ray counts relation with respect to the distance between source and detector

To use both magnifications effectively, one has to optimize all the parameters simultaneously. Thanks to a near-ideal point source used in the cited system, we are given the opportunity to move the detector and source towards or away from one another to change the pixel size while still maintaining the resolution. Geometrical magnification can help to decrease pixel size by a factor of 10 in addition to the magnification offered by the detector which is yet another option to be tuned.

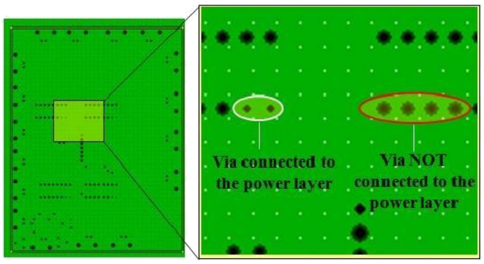


Figure 3: Layout of an internal layer.

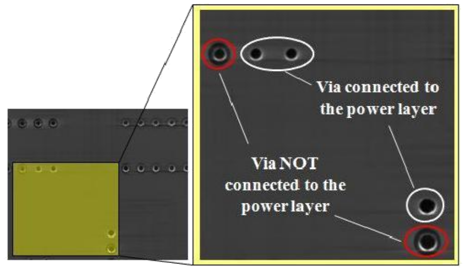
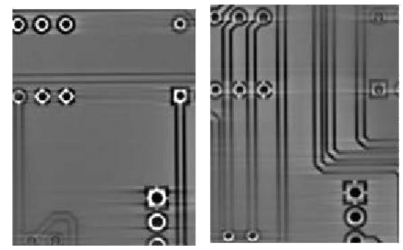


Figure 4: Virtual slicing of internal layer.



(a) (b)

Figure 5: Reconstructed (a) top and (b) bottom layers

Combining the two magnification types, one can choose any value between 0.3 to 62 microns for the pixel size. Each detector in turn has a specific number of pixels (an array of about 1000 by 1000) which defines the field of view for imaging. However, there is a trade-off. Smaller pixel size demands the detector to be positioned relatively far from the source, thus reducing the number of X-ray counts detected by the detector. Based on the principles of wave propagation, wave power is inversely proportional to square of distance from wave source. In order to get a clear image, one has to obtain 2D projections with more than 5000 X-ray counts. Therefore, to maintain such X-ray count values, the exposure time and total scanning time must be increased. In addition, the window size decreases with smaller pixel size.

The same concept applies here. The diagram in Fig. 2(a), shows the effecting items on the imaging parameters and Fig. 2(b) shows the relation between the measured detector distance and X-ray counts as it moves back. The values for distance and X-ray counts are normalized based on the maximum value for each to better show the dependent behavior of these two parameters.

A four layer custom board is first used as a proof of concept for our tomography on PCBs and then the same process will be used to do reverse engineering on a commercial Xilinx Spartan-6 starter board. Both PCBs are shown in Fig. 1(a) and Fig. 1(b) respectively.

To make sure that we can see our features on the board, we have selected a fine pixel size which gives us enough image quality. After several rounds of optimization for tomography parameters the values presented in Table I are selected. Tomography window size has a direct relation with the pixel size. The detectors on Versa 510 are an array of 1000 by 1000 pixels. This will give us an area of about 5 by 5 cm for each tomography set with the parameters in Table I. In order to do a complete tomography on the custom board (10 by 15 cm) in one session, a raster scan is performed on 6 different areas to cover the entire board. The process is completely automated after setting the parameters, and can be performed without the need for oversight. Note that the same process and a very similar set of parameters should be widely applicable to most PCBs.

Custom Board Tomography

For the four layer custom board (Fig. 1(a)), all traces, connections, and via holes are clearly captured. In order to check the effectiveness of the tomography the results are compared with the board design files previously used to print it. The board includes a front side, backside, and two internal layers. The internal layers correspond to power and ground. The via holes are connecting the traces on two sides of the board and are also connected to either power or ground layers. This is presented in the design layout in Fig. 3.

Table I. X-ray Tomography Parameters for PCB

Tomography parameters	Scan
Pixel size (μm)	49.2
Window size (μm)	49520
Detector	4X
Source distance (mm)	204.2
Detector distance (mm)	80.1
Exposure time (s)	1.2-7.2
Number of projections	3201
Total tomography time (hr)	4.23

The 3D image of the board is reconstructed using a combination of thousands of virtual 2D slices. These slices can be viewed and analyzed separately. The thickness of each of them is same as the pixel size (approximately 50 micron). In Fig. 4, one slice is demonstrated which shows the information of the internal power layer. Obviously, a better resolution or smaller pixel size will give us better image quality which can result in an easier image processing effort. However, one also has to consider that a better image will increase the costly X-ray scanning time and data size. These two parameters are considered as the controlling factors for the final PCB reverse engineering process.

Comparing the tomography results and the design layout of the board (in Figs. 3 and 4), one can see a clear difference between the via holes that are connected and those which are not connected to the internal layer. The soldering material, which provides connection of the via holes has high density and results in white contrast for the pixels. On the other hand, when there is no soldering material and no connection the isolating material between the via hole and the layer has lower density and results in dark contrast for the pixels. The same principle will let us detect the traces on the side layers of the board due to the attendance of copper on the traces as is shown in Fig. 5.

Xilinx Commercial Board Tomography

The imaging process described above clarifies the accuracy of non-destructive X-ray imaging to acquire structural information of a PCB. In the next step a commercial PCB, Xilinx Spartan 6 is chosen to be scanned and reverse engineered. This a 6 layer PCB with a complicated map of traces and joint connections on different layers. The same tomography parameters have been used for this PC. In our first imaging attempt, the board was scanned with all the components mounted on it. Most of the components such as resistors, plastic switches and ports are low Z material in the periodic table which does not cause any effect during the scanning process. However, there were also some of the components such as the soldering material and the metal ports which created artifacts in the reconstructed images. These effects appear as noise in the image, which can make it difficult to set up an automated reconstruction process. In order to solve this problem, we detached the components from the board using a hot air gun. The soldering material will also be melted down during this process. Then, imaging was performed again with improved results.

Image Stitching and Total Board Reconstruction

The entire width and length of a PCB board is much larger than the field of view of a single tomography. Yet, multiple imaging sessions not only increases the time and cost associated with imaging, but also creates errors associated with mounting and alignment. In our approach, X-ray imaging was done in one session as follows. Coordinates of each scanning region were preprogrammed and the scanning was then performed at each region of the board in order. At the end, the data from each region was stitched together to form the complete PCB.

Firstly, in order to ensure enough information is available for alignment, scanning was performed with 15-20% overlap between neighboring areas. This portion was then used to align surfaces together. The alignment process is based on Iterative Closest Point (ICP) algorithm [15]. This algorithm operates in the following iterative fashion:

1. Corresponding points in the neighboring scans are associated together based on the nearest neighbor criteria.
2. A transformation is estimated to minimize the mean square distance between the reference point cloud and the target one.
3. This transformation function (combination of translation and rotation) will be iteratively revised to best match the target cloud to the reference.
4. As a result of the previous step, there may still be some artifacts as a result of different histograms for each scan having different global minima and maxima. Some of the parameters, such as room temperature, accuracy of source power, etc., can cause the contrast or histogram changes during the tomography on different areas. For example, since the tomography is automated and will be run through the day and night, the temperature in the room will change accordingly. The contrast for every image has to be adjusted based on the other one during the stitching process. This will help to get a similar histogram for the images for each and every separate scan. A scaling process is then applied on all the areas by imposing a global minimum and maximum intensity value for the entire data set. These values are obtained by choosing the smallest minimum and largest maximum value among all stitched scans.

Image Segmentation

Although reconstructed 3D images contain valuable information, they cannot be used directly for fabrication or elaborate quantified inspection. A series of image processing steps are necessary to transform the *image* to a *computer-aided design (CAD) system* file which is a prerequisite for fabrication. In particular, to print circuits on the board, Gerber files are generated for each layer which are 2D binary CAD files containing geometric information.

The most critical step for the transition from a 3D X-ray image to a Gerber file, is *image segmentation*, that is assigning labels to each pixel (or in the case of 3D, each voxel) to extract point cloud (x, y, z) information. Efforts have been made in the past to perform image processing on images of PCBs for the purpose of inspection or reverse engineering of PCBs. [8-10]. In [8], defect characterization in PCBs have been achieved using subtraction and elimination process. The technique is limited to simple defects and physical fixtures are used for alignment purposes. In [9], series of morphological operations such as erosion, dilation, etc. are utilized for segmentation but lacks automation and after the proposed process the images are not converted to CAD files for recreation. C. Koutsougeras et al. [10] applied an automatic Verilog HDL Model Generator, which includes 2D image processing technique that is used to identify the components and their connections at much lower resolution and lacks information of the internal layers.

Here we propose an automated step-by-step algorithm (shown in Fig. 6) which can be utilized for any 3D data of the boards regardless of the imaging modality, board feature complexity, and number of layers.

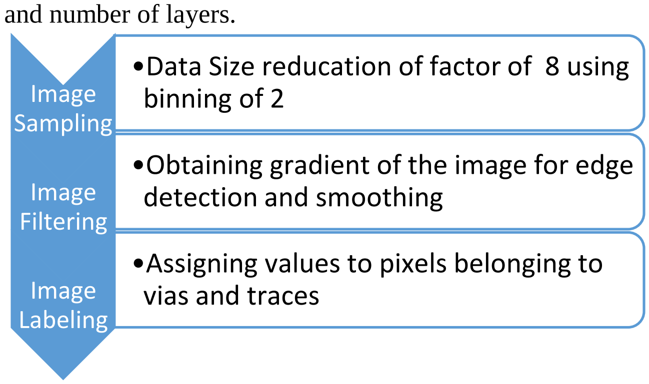
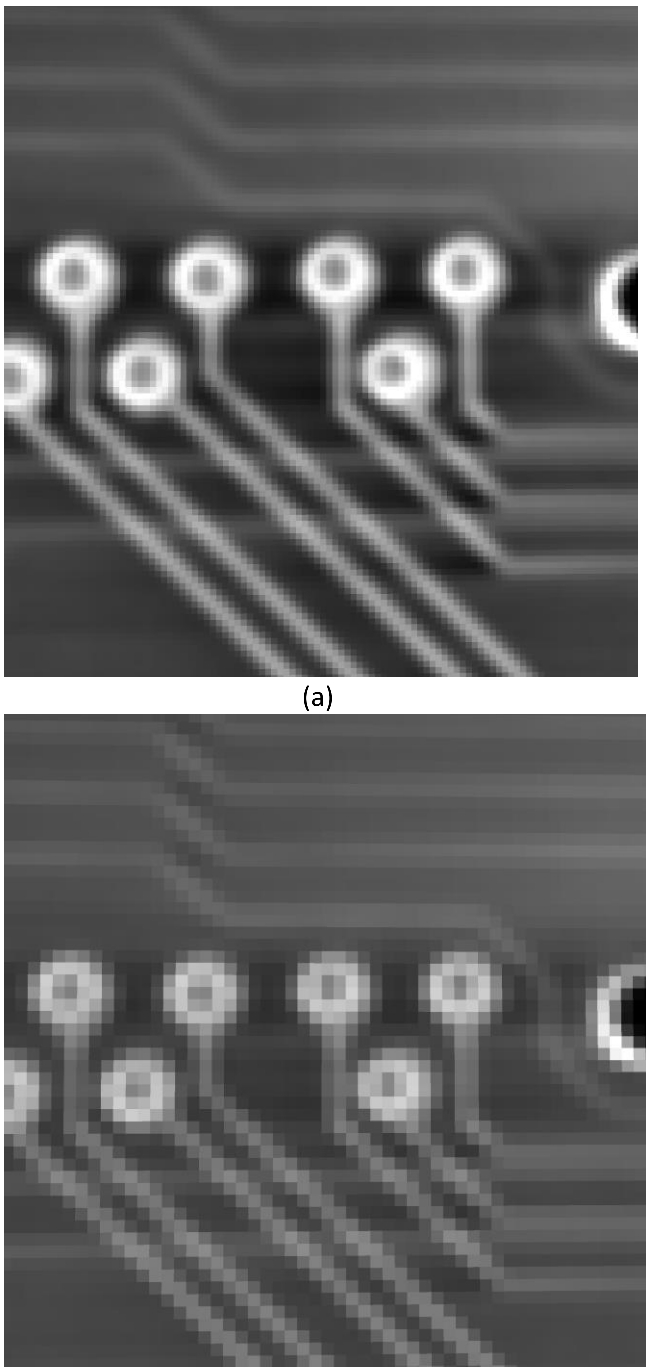


Figure 6. Image processing algorithm

The first step, *image sampling*, is deemed critical when the data size is relatively large as in this case with X-ray tomography data. For instance, the complete data set of the Xilinx board has a file size exceeding 60 GB. Sampling shrinks the dimensions of the original image grid by merging neighboring pixels. Though images may lose sharpness, using a binning of 2 can reduce the file size by a factor 2^3=8 which make the data more manageable for further processing. This process has only been used if the consequent blurring of the image doesn't make accurate segmentation impossible.

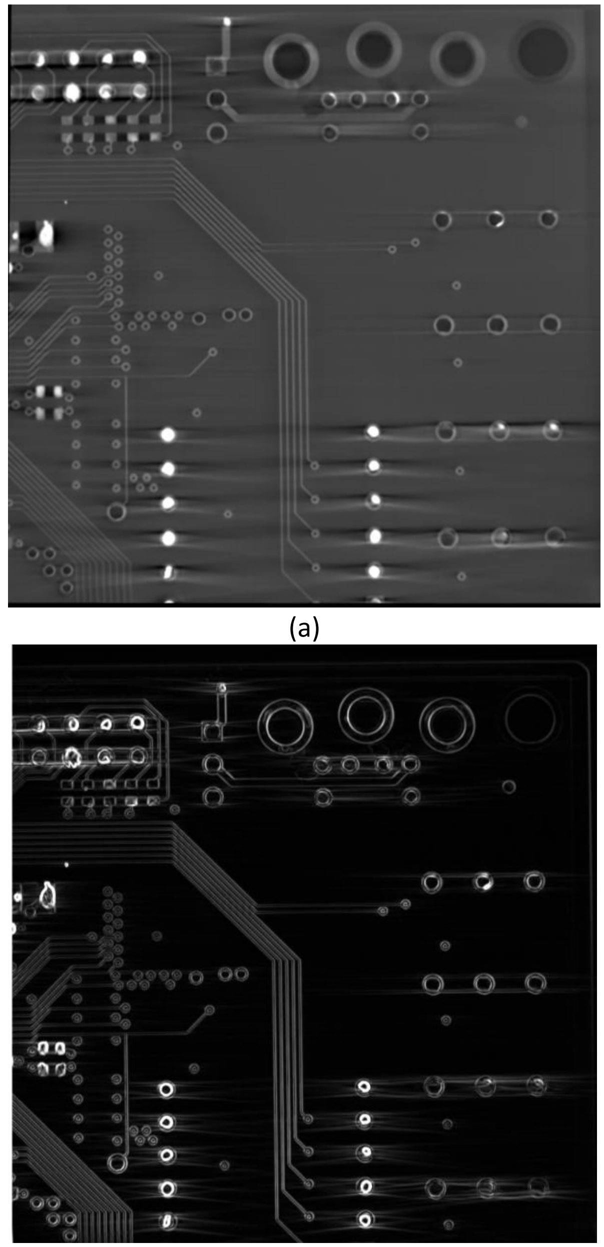


(a)

(b)

Figure 7. Image binning 2 (a) and 4 (b)

Fig. 7 shows the effect of binning on the quality of data for extraction information on vias and traces. Fig. 7(a) is image with binning 2 where traces and vias are still kept at very high quality for feature extraction. On the other binning 4, shown in Fig. 7(b) clearly shows loss of clear ages and pixilation of the image.



(a)

(b)

Figure 8. X-ray images (a) before and after (b) application of 3D Sobel operator

The next step is *filtering the images* to remove different inevitable artifacts in the 3D data. For example, due to the presence of materials with radically different X-ray absorption coefficients there are several location with saturated illumination (as illustrated in Fig. 8 (a)) Also, as the X-ray penetrates through the sample, it loses some of its energy. This phenomenon is known as beam hardening. Beam hardening can insert false image contrast within a same material making the process of labeling difficult. We have used a Sobel Algorithm to highlight the edges corresponding to traces and vias while smoothing the rest of the image. The Sobel-Filter is an edge detection filter which estimates the gradient of an image using central difference. It convolutes the image with a 3 by 3 by 3 kernel (equations 1a and 1b) in all proper directions.

$$\begin{bmatrix} -1 & -3 & -1 \\ -3 & -6 & -3 \\ -1 & -3 & -1 \end{bmatrix}, \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \begin{bmatrix} 1 & 3 & 1 \\ 3 & 6 & 3 \\ 1 & 3 & 1 \end{bmatrix} \qquad \text{Eq. 1a}$$

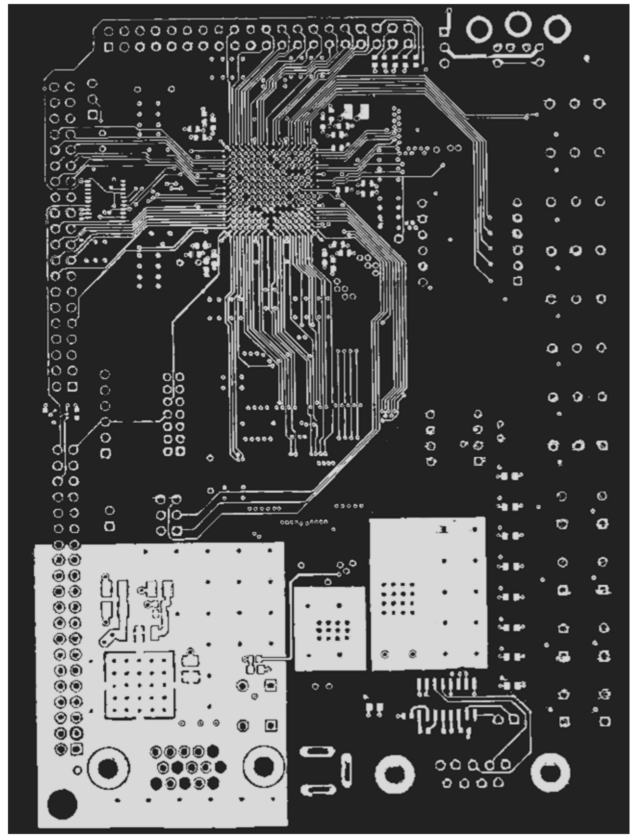
X-1 X X+1

$$\frac{\partial f}{\partial x} = \frac{f(x+1) - f(x-1)}{2} \qquad \text{Eq. 1b}$$

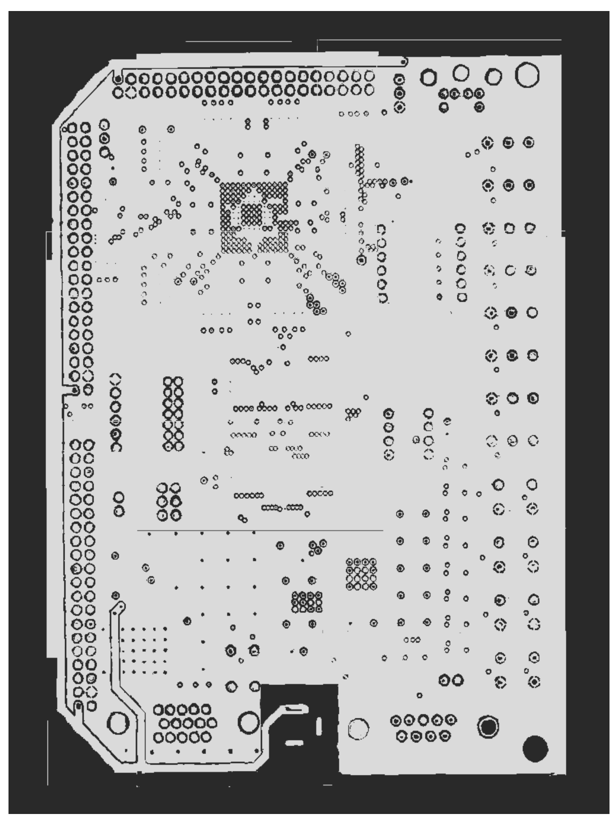
Note that the kernel in X direction has been provided above as an example. The Y and Z kernels can be simply obtained by rotating the kernel in the appropriate direction.

The filtered images are finally ready to be *labeled*. There are different techniques that can be used to segment/label including TopHat [11], watershed, thresholding [12-13], and several others [14]. Simple binary thresholding merely replaces each pixel on an image with a 0 or 1 (black or white) depending on the logical operation on the intensity of the image (i.e., if intensity < predefined threshold replace with 0, else replace with 1.) However, this simple method cannot be used for the 3D data of the boards as locations belonging to traces and via have different image intensity at different location of the image. This issue is further compounded by stitching, which adds more segments to the image with different intensity values of the same material. Therefore, we have used *localized thresholding* where image is broken into different segments which are not overlapped. In each segment, a limited range of the histogram will be selected locally. This will be according to the pixels contrast of the via and traces. Once the histogram range is selected, only the trace and via will be selected from the image when a brushing tool paints the pixel (assign values to pixels) as it scans all over the image.

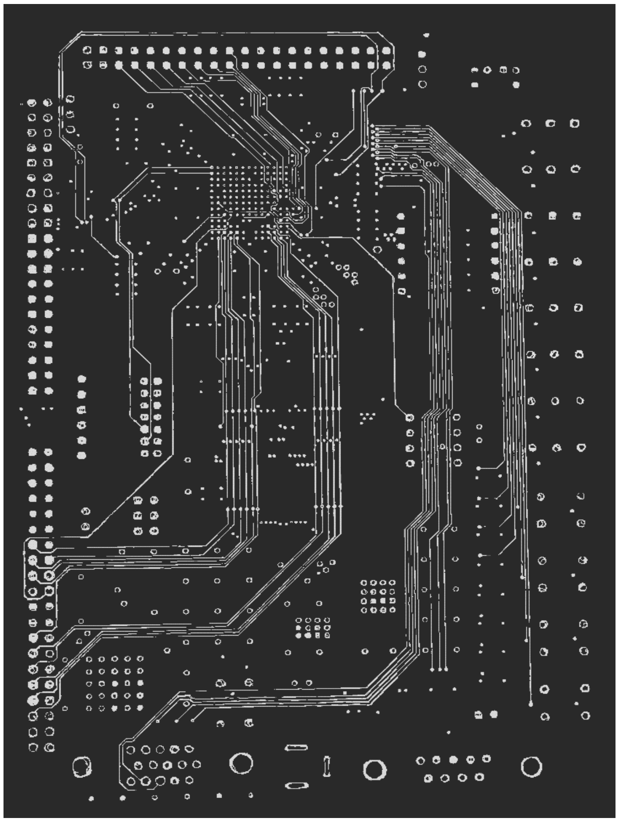
Fig. 9 shows the outcome of the process on all layers of the board. Although some of the details are not clear in the presented figures, this is due to limitations of image quality as a snap shot from a CAD file and to stay in the size limit of the total file size. The original CAD files indeed present all the details as one zooms in.



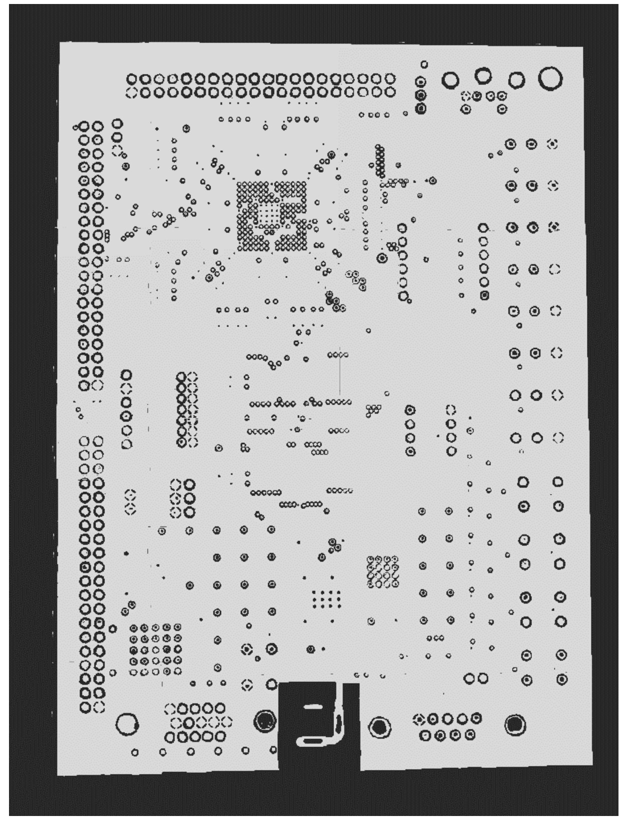
Layer 1



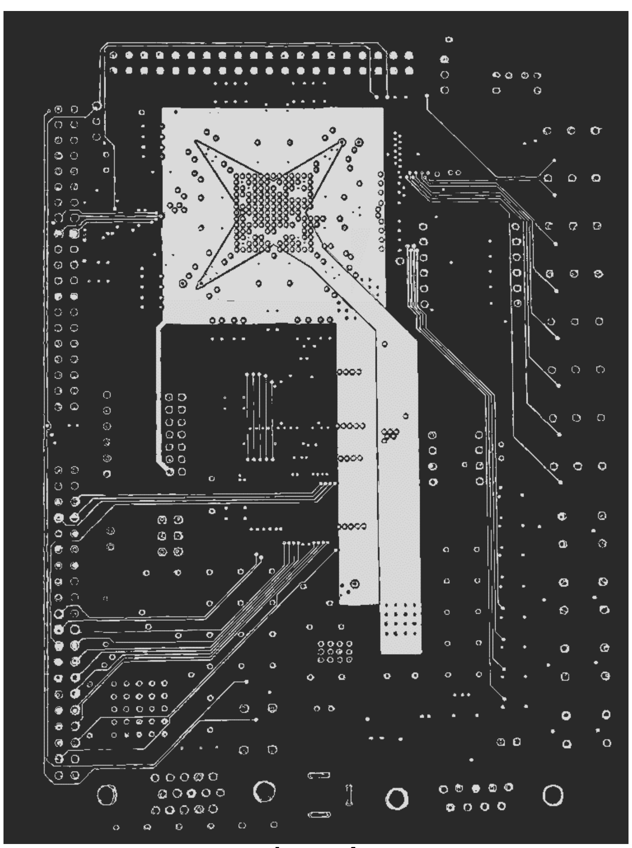
Layer 2



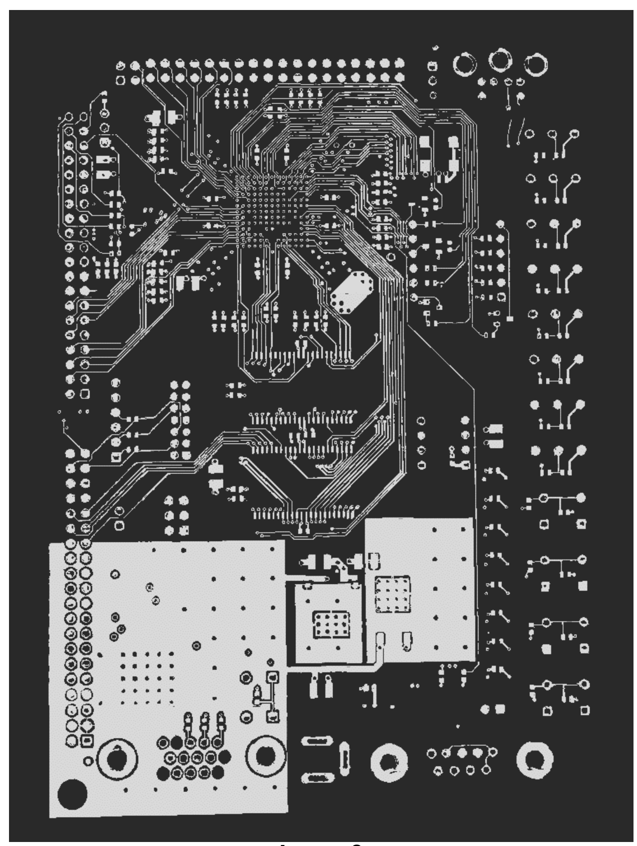
Layer 3



Layer 5



Layer 4



Layer 6

Figure 9. Segmented layout (point cluster) of six layers of PCB.

Lessons Learned to Develop Countermeasures

The proposed approach can significantly reduce the time, cost, and manual effort associated with reverse engineering. Though further efforts have to be made to duplicate functionality (firmware and software), the described method provides us with the entire geometry and 3D internal structure. Although very beneficial for honest reverse engineering obsolete designs where data sheets are no longer available, the portability of this technique is alarming. Here are the lessons learned from this research:

1. Non-destructive and fast imaging of multi-layered PCB systems are possible using X-ray computed tomography.
2. Although X-ray can penetrate through most materials used in PCB systems, there is always a challenge in feature recognition once a low density material is located next to high density material.
3. X-ray is in fact the emission of high energy photons. Although one has to note in case electrical components are on the board during the tomography, long X-ray exposure might cause damage or ionization on some of the chips. This can be also used as an external source to harvest energy to create a countermeasure structure.

We introduce concepts from the lessons learned above, to prevent reverse engineering in critical applications.

The *first class of countermeasures* is application of X-ray sensors that can react to X-ray exposure. This class of countermeasures have two subcategories of indirect and direct methods.

1) **Indirect:** Materials such Zinc sulfide are sensitive to X-ray and emit light upon exposure to X-ray or electron beam. Light sensitive films can also detect the light and generate current in very small scale values. Using the combination of Zinc sulfide and photodiode, one can implement an X-ray sensor in the system to store the history of the devices exposure to high energy X-ray photons and/or react destructively when the exposure exceeds a certain limit. This allows for limited X-ray inspection as a common practice for authentication, but negates the chance of thorough reconstruction.
2) **Direct:** In direct mode, X-ray photons are directly converted to electrical charge which can be used to alter information in the device. These type of sensors are fabricated from solid state material such as silicon [18]. The amount of exposure and the X-ray power defines the output of the sensor. Depending on the amount of energy harvested from the sensor, one can use that to store exposure information in the device or use it as an anti-reverse engineering sensor as stated above.

Although sensors will help to see whether or not the device has been attacked, they may not prevent the entire information piracy. The *second class of countermeasures* addresses this issue through materials that have excessively large X-ray attenuating coefficient. X-ray can penetrate easily through the general PCB material and create clear 3D images with high signal-to-noise-ratio. Adding high density material such as Zirconia powder, which has a very high X-ray attenuation coefficient, will reduce the X-ray transmission amount through PCB and will result in much lower signal-to-noise-ratio. This can be used in a specific pattern in between several layers. Thus, indeterminate information will make the transition to a CAD file almost entirely impossible.

Conclusion and Future Work

In this paper, we have presented non-destructive reverse engineering by x-ray imaging of a simple, custom PCB and another, more complex commercial Xilinx Spartan-6 starter board. The netlist of components and connections were extracted as a point cluster with xyz information from the images using advanced image processing techniques. These type of files can be directly converted to DXF or GERBER files which are compatible with circuit printing machines. We will continue the study to develop a software where the X-ray images are imported and the final netlist is generated as output in a completely automated fashion. Since RE could lead to IP theft, piracy, cloning, etc. of PCB products, we have also proposed countermeasures which might mitigate the threat of the proposed technique. We hope that this paper raises awareness of the current-state-of-the-art techniques and provides motivation for the development of additional low-cost and robust anti-RE techniques.

Acknowledgments

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