Non-Destructive Bond Pull and Ball Shear Failure Analysis Based on Real Structural Properties

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Abtract: *Bond pull testing, a well-known method in the failure analysis community, is used to evaluate the integrity of an electronic microchip as well as to detect counterfeit ICs. Existing bond pull tests require that the microchip be de-capsulated in order to obtain physical access to the bond wires in the IC package. Bond pull analysis based on simulation and finite element methods also exists but relies on the original model for a bond wire from a CAD design. In this work, we introduce X-ray tomography imaging with 700nm imaging resolution to acquire the 3D geometry details of bond wires non-destructively. Such information can be used to develop more accurate models for finite element analysis based on real size and structure. Therefore, one can test the bond wire strength as a proof of concept for virtual mechanical testing and counterfeit detection in microchips.*

Keywords: Bond Pull; Non-Destructive Evaluation; Finite Element Modelling; 3D X-ray Tomography

1. Introduction

There are different methods to connect a die to the lead frame, but according to [1], [2] more than 95% of such connections are based on wire bonding. Bond wire integrity is a critical parameter in the reliability of a microchip. For example, military-grade microelectronic components need to perform under higher thermal and mechanical loads which may impact bond wire integrity and, eventually, chip performance. Thus such chips require higher standards for bonding.

In the industry, the two most prevalent tests used to capture tolerance of chips to harsh environments are bond pull and ball shear [3], [4]. These tests require that the testing tools have clear access to the bond wires, which means the chip has to be de-capsulated either locally or entirely. Chemicals such as acids are typically used for removing the entire package, but local de-capsulation may also be performed with laser- or plasma-based methods. Once the access to bond wires is created, one can perform destructive or non-destructive tests to detect damage to bond wires. None of the chips subjected to either of these test methods will be suitable for onsite usage afterwards [5], [6].

In the destructive test, force is applied on the bond wire until one of the following failures occur: wire break, bond pad peeling, wire neck break, or ball shift. In the non-destructive test, however, the force will not exceed 90% of the designed strength of the bond wire. This can result in other types of failure which we consider out of the scope of this paper. For more details, we refer the reader to [7], [8].

Regardless of the choice, there are several disadvantages to either test approach: 1) the package should be entirely or locally de-capsulated, which is costly, time-consuming, and requires additional expertise; 2) each wire can be used for only one physical test; 3) fatigue analyses require very long testing times and a controlled experiment environment; and 4) the effect of mechanical load (e.g., pull force) is exerted only on one wire at a time.

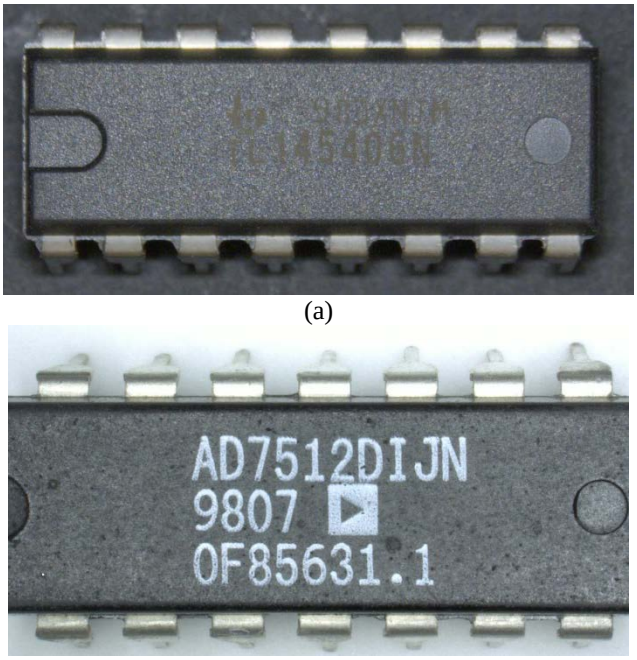
Such disadvantages encourage research into the development of virtual methods—in particular, finite element modelling (FEM)—to run these tests in a way that will save time and money [8]. Although FEM can help to speed up the testing procedure, any solution requires accurate information for initial and boundary conditions in an FE model. Such information can only be acquired from the geometry and structure of real test samples. However, since it is not easy to gain physical access to all of the internal structure, the final 3D model is always a simplified version of the real model.

In this paper, we introduce a new approach based on 3D X-ray tomography in order to provide enough information to simulate a real bond-wire model non-destructively, i.e., without the need to physically de-capsulate a microchip. In prior work, the authors have investigated reverse engineering [9], [10] using X-ray tomography and image segmentation [11]-[13], which has set the stage for our research. The rest of the paper is structured as follows: Section 2 talks about the methodology of this work, which is based on a case study; Section 3 describes the X-ray tomography setting and parameters; Section 4 describes the post-processing algorithm and how to generate CAD files from X-ray images; Section 5 talks about how the CAD file is imported into an FE platform and how the model is set up; Section 6 presents the stress and

displacement results for bond wires; and Section 7 concludes the paper with plans for future work.

2. Methodology

We introduce this method using a case study in order to make it easier for readers to follow and understand the details. Among the chips available in our lab, two random chips with bond wires have been selected for the analysis—a Texas Instrument TL 145406N microchip (as seen in Figure 1) and the AD7512DIJN by Analog Devices. However, the whole procedure is entirely independent of the chip type and not specific to these two samples. In addition, the same concept can be applied on ball grids for shear test, which will be investigated in future work.



(a)

(b)

Figure 1. 3D X-ray (top) and chip profile image (bottom) of a) Texas Instruments TL 145406N and b) AD7512DIJN

3. X-ray Tomography

In order to create an accurate FE model of bond wires, one needs to acquire accurate information from the real test samples. Here we introduce X-ray computed tomography to gather the structural information of bond wires with a resolution of down to a few microns. We have used a GE Phoenix system for tomography. The GE Phoenix is a dual tube system, which is capable of scanning high- and low-density material.

The Phoenix Vtome X M CT has a 180 KV Nano focus tube and a 240 Kv Micro focus tube. Both tubes are located inside the system, and they can move around automatically based on the required imaging resolution and sample type, and can align precisely with the detector to minimize the center-shift effect. This system has a dynamic DXR digital detector with 2024×2024 pixels, and is also equipped with GE's scatter/correct technology which minimizes the scatter artifacts from the reconstructed volumes and enables users to better extract the internal features compared with conventional tomography.

Tomography parameters for the testing chips are shown in Table 1 and were based on few rounds of tomography in order to optimize the values and get the highest transmission and lowest noise in the images.

Table1. Tomography parameters for microchips

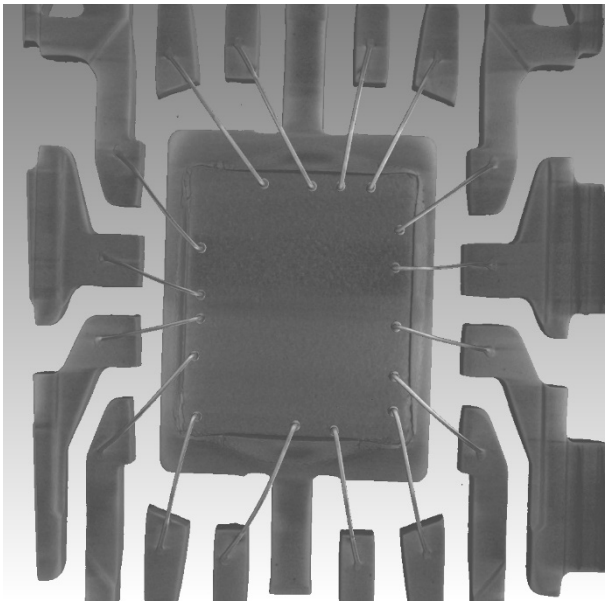
	TL 145406N	AD7512DIJN
Magnification	35.94	37.98
Voxel size (µm)	5.56	5.26
Focus-Object-Distance (mm)	22.39	21.2
Focus-Detector-Distance (mm)	805.22	805.22
Number of projections	1200	1200
Source voltage (kV)	200	200
Source current (µA)	25	25

Figure 2 shows the reconstructed 3D image of these chips. Datos software from Phoenix has been used for the 3D reconstruction (Radon transform is the basic transform function of reconstruction algorithms similar to many other systems). As seen in Fig. 2, the geometry and the internal structure of all bond wires can be very well captured using the non-destructive X-ray tomography. A major challenge in tomography is imaging artifacts, but scatter/correct technology in this system helps to reduce them in chip images.

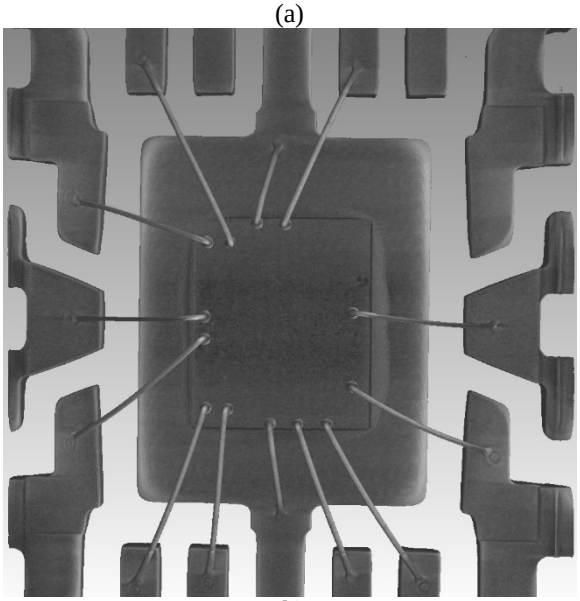
Material properties are available from the chip datasheet. These two sets of information, the material properties and geometry of bond wire, will be enough to create a finite element model and analysis the strength of bonding wires.

4. Image Segmentation

In this section we will discuss how we converted the acquired 3D image from .pcr format (which is the standard format for reconstructed images of GE X-ray products) to a real finite element model. Once the



(a)



(b)

Figure 2. Non-destructive 3D image of the test chips using X-ray tomography a) Texas Instruments TL 145406N (chip1) and b) AD7512DIJN (chip2)

FEM is ready for analysis, one can analyze the model with any type of solvers, such as Autodesk simstudio, ABAQUS, COMSOL, NASTRAN, etc. We refer to this as the reverse-engineering step of this work.

It is critical to note that imaging resolution or detectability is the only limitation for the accuracy of the reverse-engineered model. Industrial X-ray CT systems currently provide a wide range of imaging resolution, from tens of nanometers up to millimeters. However, there is always a relationship between the sample size and the optimal imaging resolution. The GE X-ray system used for this paper can acquire high resolution images down to 1 micron. Although this can detect a lot of cracks causing failure in bond wires, it would be almost impossible to detect smaller cracks with this system. Ultra CT systems, which are not yet as popular as the micro CT systems, can provide down to 50 nm resolution; however, the sample size needs to be really small and in the range of few hundreds of microns since the X-ray energy and power are only below 10 KV. Therefore, an ultra CT system does not represent an option for non-destructive bond wire analysis at this time.

As proof of concept, we will perform a finite element analysis on the bond wire of the chips mentioned in Figure 1. We will only show the bond pull in this paper due to the time limitation; however, any other types of similar tests—such as thermomechanical tests, fatigue, multiphysics analysis, vibration, impact test, etc.—can be modeled in the same way using different solver packages.

X-ray 3D images are initially in the .pcr format. This format is similar to .tiff files and is considered an image. It is not a CAD model that can be analyzed without additional post-processing.

We have used VG Studiomax 22 from Virtual Graphics group for the first step in post-processing. VG is a powerful image processing package and is widely used for image processing, filtering, segmentation, etc., on various types of samples, such as semiconductors and electronics, fossils, and more. In the following, we have briefly described the segmentation process:

1) Region growing (flooding) algorithm is used to segment each bond wire separately in a semi-automated fashion based on the reconstructed 3D X-ray image histogram. Although this step can be done for all bond wires at once, the accuracy will be lower due to the noise (coming from beam hardening or center shift) in the images, which is common for most of CT images.
2) Once the bond wire is segmented, we refine the region of interest (ROI) according to the local gray-value gradients. This step eliminates sharp edges in the surface, which are mostly due to the noise in the image and are difficult to mesh during the finite element analysis.
3) Once the whole bond wire is segmented, the model is exported as an .stl file, which is standard format for CAD models and can be easily imported to FE packages or into a 3D printer.

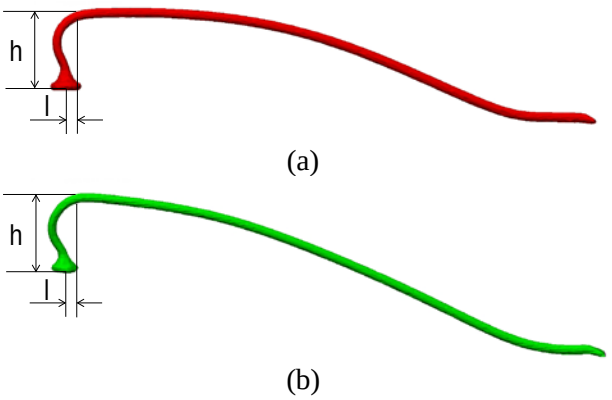


Figure 3. Segmented files for single bond wires a) TL 145406N and b) AD7512DIJN

Once the .stl file is ready, it can be imported into Autodesk Simulation or Autodesk SimStudio for further analysis or modification. We have imported our .stl files into Autodesk Simulation for further analysis, as seen in Figure 3. Other geometrical properties of bond wires—such as loop-part (l), loop-height (h), and wire diameter—can be also measured virtually based on such results.

5. Finite Element Model Preparation

According to the literature, there are three different types of bond wire failures:

1) Bond lift off from pad metallization on ball bond or stitch side.
2) Wire break at bond heelcrack or neck break on ball bond or stitch side.
3) Wire break that occurs on any place other than the previous two cases.

As one can see from the description of the first type of bond wire failures, bond lift is about the reliability of the wire attachment to the die and pad and not about the wire itself. Details about ball bond or the wire attachment to the die are currently very difficult to detect, particularly in newer node technology, since the die thickness is below 1 micron and is too thin for the current X-ray technology to capture. However, there is no other limitation in applying the proposed technique and analyzing the other failure modes. This will be the only limitation of this technique, though this is technically a limitation of the imaging and not of the proposed concept, which is the main focus of the paper. On the other hand, the industrial X-ray CT technology is growing very fast and may be able to resolve the smaller features in near future. As a result of the above limitation, in this paper we shall focus on the wire-break and neck-break failures only.

A thorough visual inspection was done on all bond wires to detect any cracks or other types of anomalies; however, there were no such defects found in our test samples. Therefore, to save time and to lower the computing costs, we have segmented two bond wires from each chip as shown in Figure 3.

Bond wire .stl files are imported into the Autodesk Simulation Mechanical 2017 software to pursue the FE analysis. The material, meshing elements, and loading conditions can be edited in this package. We have selected copper for TL145406N and aluminum for AD7512DIJN. After selecting the material, the next important step for an accurate FE modeling is to mesh the model in an effective way so that critical regions are covered with an optimized number of elements. Due to the irregular shape and geometry of bond wires, we have selected tetrahedral elements for meshing. Tetrahedral elements are compatible with third-party Finite Element Analysis packages, but hybrid brick shapes from Simulation Mechanical are not compatible with some of the other programs. The four-node tetrahedral element also provides a uniform mesh for 3D analysis since such elements can easily sit next to each other and cover the whole area. There are no midside nodes included for this element, and the second order integration is selected as default. More information in regard to the meshing for all four models are presented in Table 2.

Table 2. Meshing elements and bond wire information

Chip type	TL 145406N		AD7512DIJN	
	Wire 1	Wire 2	Wire 1	Wire 2
Mesh size (µm)	6.1	6.8	16.1	18.09
Total elements	40468	34195	10225	5154
Total nodes	9855	8526	3047	1664
Loop-part (µm)	30	29	72	46
Loop-height (µm)	179	183	254	257
Diameter (µm)	26.4	23.7	31.2	30.3

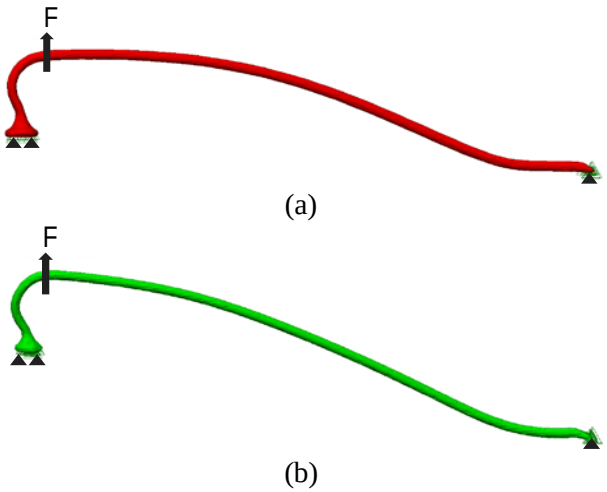


Figure 4. Initial and boundary conditions for the bond wires FE analysis a) TL 145406N and b) AD7512DIJN

As seen in Table 2, we have first selected fine elements as small as about six microns, which is about one-fourth of the wire diameter for the first chip, TL1245406N. Since there are no defects in the wires, we have used larger elements for the second chip, AD7512DIJN. Once wires are meshed, boundary conditions and loading can be applied.

Figure 4 shows the location where we applied the loading force of 1 cN. We chose the peak of the wires because this is where bond wires are most commonly tested for physical tests. Fixed boundary conditions on both ball-bond and stitch-end sides are also added to the model. This means the model at this stage will only include the two types of failure mentioned earlier.

A more detailed version of the bond wire model with simulated contact between bond wire and lead frame information can include the first failure mode as well, but this was not developed in this work due to time limitation.

Once the model is fully prepared, Autodesk has two solver options to offer: Simulation Mechanics and Nastran. We have used the Simulation Mechanics solver for this paper, and the results are presented in the next section.

6. Results

Physical bond-pull testing results in the failure of the bond wire itself, which means the chip is no longer functional. There are standards for the loading force in bond-pull testing depending on the chip type and size. Results in this section present the critical regions where the failure has the greatest likelihood of occurrence. This can be used to optimize the design or wiring process to minimize the critical regions.

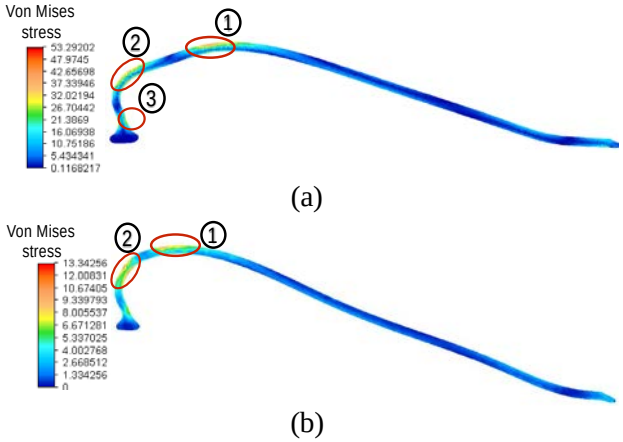


Figure 5. Von Mises stress distribution (N/mm^2) for a) TL 145406N and b) AD7512DIJN

Here we present two important sets of results for each wire, which can provide enough information to decide whether or not the wire will fail under its loading conditions.

We will show the results for one wire from each chip to reduce the redundancy, since results appeared similar for each chip as one might predict. Since both aluminum and copper are ductile materials, we have used Von Mises stress distribution and displacement magnitude to show the changes. These parameters have been used widely in literature for linear structural analysis. Figure 5 shows the displacement magnitude distribution, and Figure 6 shows the Von Mises stress distribution for the first bond wire in the two different chips after the load is applied. Stress estimations are calculated based on a stress-to-nodes method. This method provides greater accuracy by using extrapolation scheme, as compared to stress calculations that are obtained by using stress inside elements. This method makes it more accurate to derive the stress values on the nodes, which is more valuable than stress estimations for whole elements. Note that displacement magnitude is a parameter greater than or equal to zero that lets us know the total distance the node has moved.

As seen in Figure 5a and 5b, two regions (points 1 and 2) are suspicious for early failure because they have the maximum value. It is also evident that in chip 1 (Figure 5a), there is a third point very close to the ball-bond end with high stress. This could be due to the non-standard shape of the wire. It has been seen in many cases that the bond wire is not generated in a standard form, and this can cause such stress

concentrations and may end to early failure as well. For the first chip, the maximum stress value is about

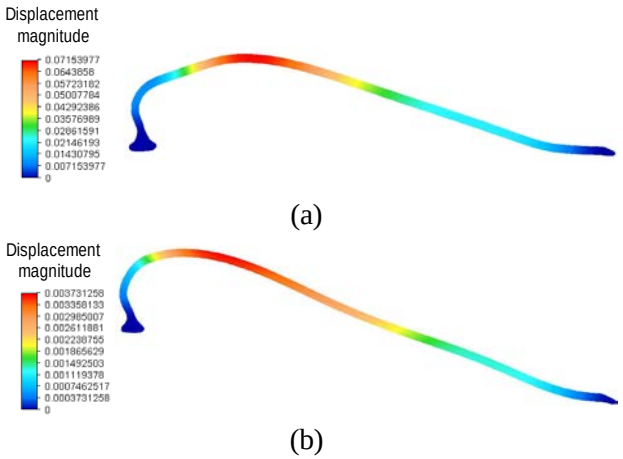


Figure 6. Displacement magnitude distribution (µm) for a) TL 145406N and b) AD7512DIJN

53 N/mm^2, and for second chip it is about 13 N/mm^2. Figure 6 (a and b) represents the displacement magnitude for both chips. The maximum displacement is about 70 microns for the first chip and 3 microns for second chip. Although stress distribution is more important for failure analysis, the displacement magnitude distribution confirms that failure is not a direct function of maximum displacement in bond wire problems.

7. Conclusion

We have introduced a novel, nondestructive method for acquiring accurate FEM models of bond wires which represents a promising alternative to existing mechanical testing procedures that rely on de-capsulation. We have shown that under optimized settings of X-ray tomography, one can obtain high-fidelity 3D images of the internal attributes of the IC. Image segmentation can result in a 3D model that is not parametrically editable, excessively large, and not suitable for feeding into FEM packages. A process for reverse engineering of the wires can significantly reduce file size, and can create a CAD file that is editable and easily transferred between software packages. A finite element analysis was shown as a proof of concept for bond pull testing and correctly demonstrates the area of stress concertation and possibility of failure. These locations conform with those obtained from experiments, which suggest that the results can be extended to more complex analysis such as fracture mechanics due to the existence of cracks in bond wires and fatigue.

Future Work

We plan to apply this method on more microchips with different internal structure, to extend this method to all types of chips, and identify additional limitations (if any exist). Also, through comparison of virtual results with real experimental results, we plan on optimizing the finite element model in terms of meshing properties, constitutive relationships, etc., to better correlate with real experimental tests.

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