Localized Growth of Carbon Nanotubes on CMOS Substrate at Room Temperature Using Maskless Post-CMOS Processing

Ying Zhou, Jason Lee Johnson, Ant Ural, and Huikai Xie

***Abstract*—Carbon nanotubes (CNTs) have been successfully synthesized on foundry CMOS substrate using maskless post-CMOS surface micromachining and localized heating techniques. The integrated heater is directly made of gate polysilicon and suspended over a micromachined cavity for thermal isolation. The synthesized CNTs are connected to CMOS interconnect metal layers without the need of any metal deposition. It is experimentally verified that the electrical properties of the neighboring CMOS transistors are unchanged after CNT growth.**

***Index Terms*—Carbon nanotubes (CNTs), CMOS, monolithic integration, nanotechnology.**

I. Introduction

THE EXTRAORDINARY electrical and mechanical properties of carbon nanotubes (CNTs) make them attractive for beyond-CMOS technology scaling and high-sensitivity chemical and biological sensors [1]–[3]. A complete system with CNTs and microelectronic circuitry (e.g., CMOS) integrated on a single chip is further desirable to fully utilize the potential of CNTs for emerging nanotechnology applications, such as smart gas sensing [4], since CMOS circuits provide advanced system control and powerful on-chip signal processing. This monolithic integration requires not only high-quality CNTs but also a robust fabrication process that is simple and compatible with mainstream foundry CMOS processes. Such CMOS-compatible integration process up till now remains a challenge, mainly due to the temperature and material limitations of CMOS technology [5], [6]. Thermal chemical vapor deposition (CVD) has been widely used to synthesize CNTs [7]–[9]. For example, Tseng *et al*. demonstrated integration of CNTs with the NMOS circuit in CVD furnace at 875 °C [10]. However, the high synthesis temperature (typically 800–1000 °C) would melt aluminum interconnect layers and deteriorate the on-chip transistors. For example, Ghavanini *et al*. reported that one PMOS transistor lost the function after the 610 °C thermal CVD growth [5]. One possible solution is to grow CNTs at high temperature first and then transfer them to another substrate at low temperature [11]–[14], but the process complexity and alignment accuracy are still concerns. Some other attempts were made to reduce the growth temperature to as low as 120 °C using various CVD methods [15], [16]. However, both the quality and yield of the CNTs decrease with reduced growth temperature.

Localized synthesis based on microheater resistive heating, first shown by Englander *et al*. [17], offers a solution that provides high temperature at predefined regions for optimal CNT growth, leaving the rest of the area at low temperature. Although localized CNT growth on various microelectromechanical systems (MEMS) structures has been demonstrated [17]–[19], the devices typically have large sizes and their fabrication processes are not fully compatible with foundry CMOS processes. On-chip CNT growth using CMOS microhotplates was later demonstrated by Haque *et al*. [20], but this approach is limited to SOI CMOS substrates and requires a complex backside bulk micromachining process. Moreover, the utilization of a refractory metal (e.g., tungsten) as interconnect metal is limited in foundry CMOS especially for mixed-signal CMOS processes.

In this paper, we report a simple and scalable post-CMOS CNT integration approach that is fully compatible with commercial foundry CMOS processes. CNTs are synthesized selectively on polysilicon microheaters embedded aside CMOS circuits using maskless post-CMOS surface micromachining and localized heating techniques. There is no need of any photomasks or shadow masks or metal deposition for achieving the localized growth and the CNT-polysilicon electrical contact. Successful monolithic integration of CNTs and CMOS is demonstrated and it is verified that the electrical properties of the neighboring CMOS transistors are unchanged after CNT growth. This work opens up the possibility of integrating CNTs and commercial foundry CMOS circuits for emerging hybrid nanoelectronics applications.

II. CNT-CMOS Integration Technique

The basic idea of this monolithic integration approach is to use post-CMOS MEMS fabrication to form microcavities for thermal isolation and to use gate polysilicon as heaters for localized heating as well as CNT interconnect. The concept is illustrated in Fig. 1(a), which shows the cross-sectional view of a device. The microheaters, made of gate polysilicon, are suspended in a microcavity on a CMOS substrate. The microcavity is created using a maskless post-CMOS microfabrication process. The required etching masks are already formed by the CMOS interconnect layers during foundry CMOS fabrication. The top view of a microheater design is shown in Fig. 1(b). There

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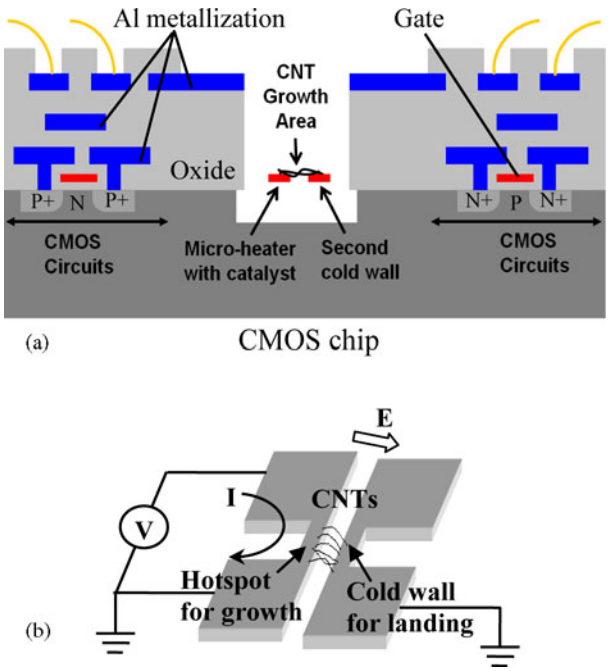

Fig. 1. (a) Schematic diagram of the device cross section. (b) Schematic 3-D microheater showing the local synthesis from the hotspot and self-assembly on the cold landing wall under the local electric field.

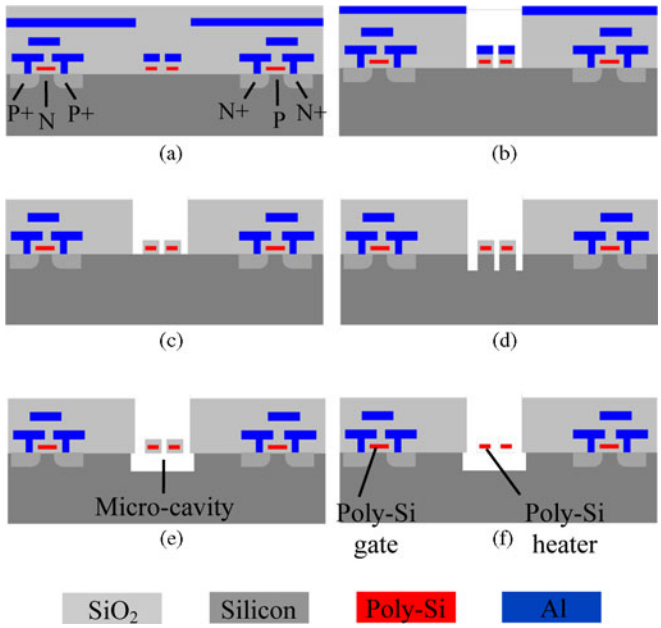

Fig. 2. Fabrication process flow. (a) CMOS chip from foundry. (b) SiO_2-dry etch. (c) Al etch. (d) Anisotropic Si-dry etch. (e) Isotropic Si-dry etch and heater release. (f) SiO_2 wet etch.

are two polysilicon bridges: one for generating high temperature to grow CNTs and the other for CNT landing. Note that there will be an electric field between the two bridges during CNT growth. The CNT synthesis is activated by localized heating. CNTs will start to grow from the hotspot (i.e., the middle of the hot bridge) and will eventually reach the cold bridge under the influence of the local electric field. The electric field helps the nanotubes to align [8] and facilitates them to bridge over. Since both the microheater bridge and the cold bridge are made of the gate polysilicon layer and they are interconnected with the metal layers in foundry CMOS process, the synthesized CNTs can be electrically connected to CMOS circuits on the same chip without the need of any clamping or connection steps.

III. Fabrication Process

The CMOS chips used in this work were fabricated through MOSIS using the commercial AMI 0.5 μm three-metal CMOS process [21]. The sizes of the investigated NMOS and PMOS transistors are $W_n/L_n = 3.6$ μm/0.6 μm and $W_p/L_p = 7.2$ μm/0.6 μm, respectively. The gate oxide thickness is 13.5 nm. The cross-sectional view of the maskless post-CMOS process flow used to create the polysilicon microheaters is shown in Fig. 2. The process starts with reactive ion etching (RIE) of silicon dioxide and uses metal-1 and metal-3 layers of the CMOS substrate as etching masks to protect the CMOS circuit area [see Fig. 2(b)]. The etch chemistry used in this step is a mixture of CHF_3 and O_2. All the required etching mask patterns are formed in the CMOS foundry processing. Next, the exposed metal (i.e., aluminum) is etched by RIE [see Fig. 2(c)], using BCl_3, Cl_2 and Ar. Then an anisotropic deep-reactive-ion etching (DRIE) of silicon is performed [see Fig. 2(d)] with SF_6 and C_4F_8 as the etching and passivation gas, respectively, to create a roughly 6 μm-deep trench around the heater. Next, an isotropic silicon etching using only SF_6 is performed to undercut the silicon under microheaters [see Fig. 2(e)], resulting in suspended microheaters in microcavities. Finally, the thin SiO_2 isolation layer surrounding the microheaters is etched away by a 6:1 buffered oxide etchant at room temperature for 5 min to expose polysilicon for electrical contact with CNTs [see Fig. 2(f)].

After the microheaters are released, the chip is wire bonded to a DIP package and coated with an alumina supported Fe/Mo catalyst [8] by drop-drying on the surface. The whole package is then placed into a quartz flow chamber equipped with electrical feed-throughs. The package is connected to a power supply using clamps. The on-chip microheater is turned on by applying an appropriate voltage (in the range of 2–3 V), which also introduces a local electric field of about 0.1–1.0 V/μm. The CNT synthesis is carried out using 1000-sccm CH_4, 15-sccm C_2H_4, and 500-sccm H_2 for 15 min. The chamber stays at room temperature all the time.

IV. Microheater Design

The microheater design is critical for successful nanotube growth. The temperature needs to reach at least as high as 800 °C for single-walled nanotube growth, and drop quickly to avoid damaging the surrounding CMOS circuits. Therefore, structural stiffness, thermal isolation, and thermal stresses must be well balanced when designing the microheater structures. The polysilicon layer is thin and its thickness varies with different foundry CMOS processes. For the AMI 0.5 μm CMOS process [21] used in this work, the polysilicon thickness is 0.35 μm. A typical heater design is shown in Fig. 3(a), which

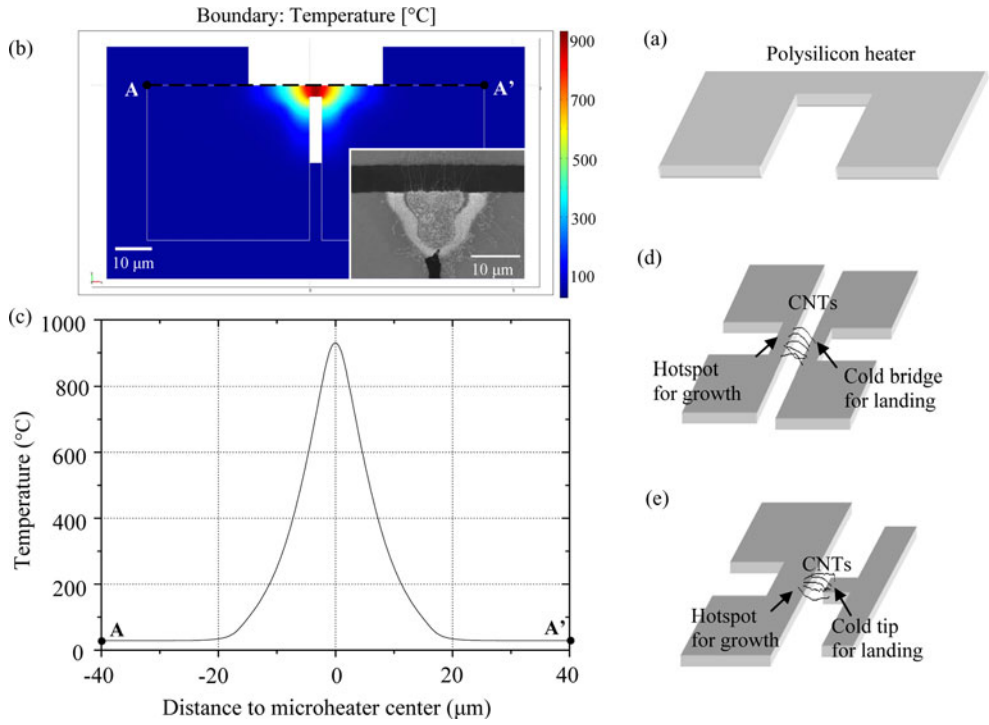

Fig. 3. (a) Typical heater design with stripe-shaped resistor. (b) Simulated temperature distribution along the surface of the microheater at an applied voltage of 2.5 V through the pads. The area of polysilicon microheater is 3 μm $\times$ 3 μm, and a thickness of 0.35 μm is chosen according to the CMOS foundry process. (Inset) SEM image of a microheater after CNT growth. (c) Line plot of the temperature along the heater [line AA' in (b)]. (d) and (e) 3-D microheater configurations with parallel cold bridge and sharp tip as landing wall, respectively.

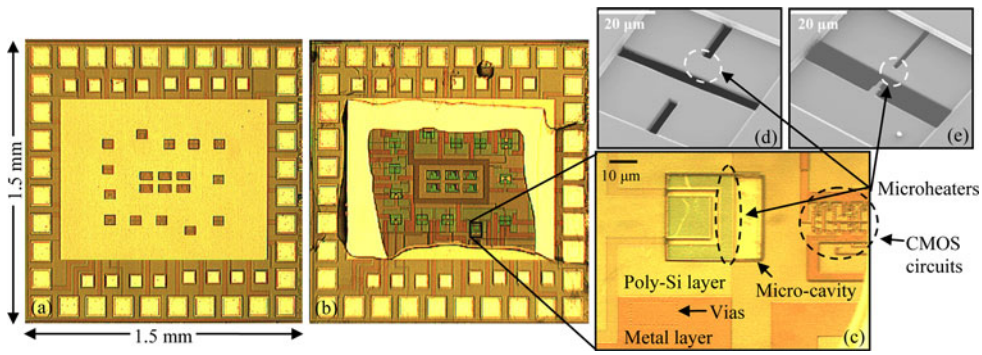

Fig. 4. (a) CMOS chip photograph (1.5 mm $\times$1.5 mm) after foundry process. (b) CMOS chip photograph after post-CMOS process (before final DRIE step). (c) Close-up optical image of one microheater and nearby circuit. CMOS circuit area, although visible, is protected under silicon dioxide layer. Only the microheater and cold wall within the microcavity are exposed to synthesis gases. Polysilicon heater and metal wire are connected by vias. (d) and (e) Close-up SEM images of two microheaters.

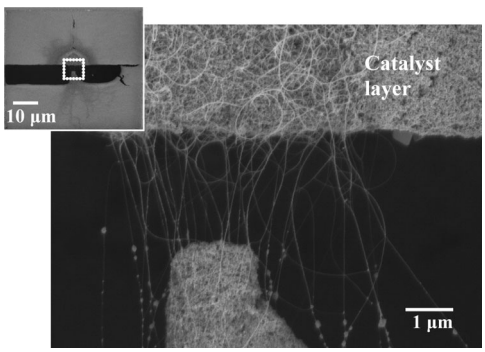

Fig. 5. Localized synthesis of carbon nanotubes grown from the 3 μm $\times$ 3 μm microheater, suspended across the trench and connecting to the polysilicon tip.

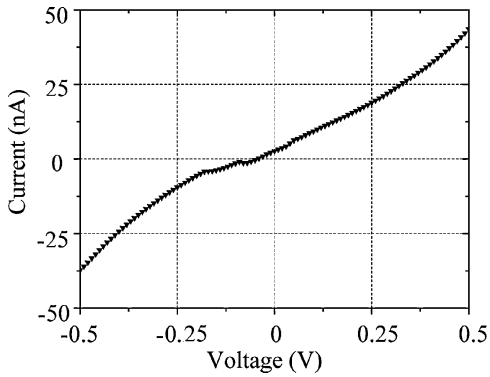

Fig. 6. *I–V* characteristics of the as-grown CNTs. The *I–V* curve is measured between two polysilicon microstructures contacting the nanotubes.

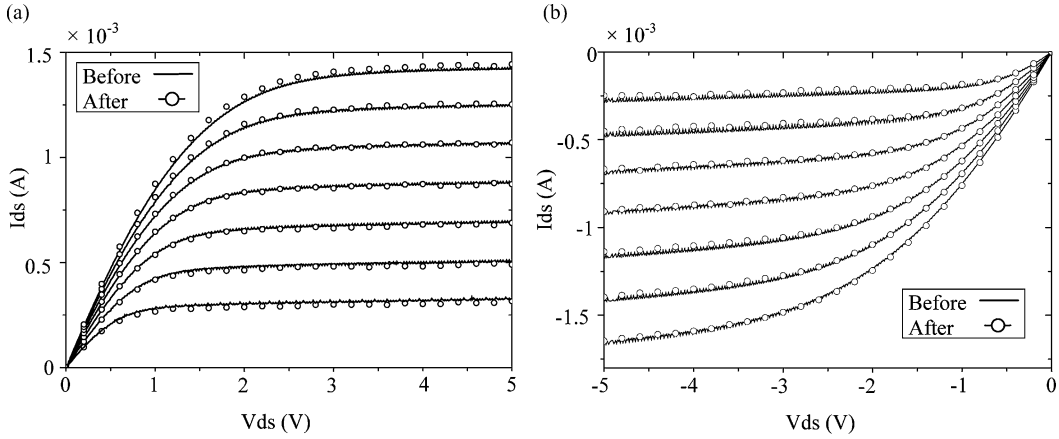

Fig. 7. DC electrical characteristics of single transistors before and after carbon nanotube growth. (a) Drain current ($I_{\rm ds}$) versus grain voltage ($V_{\rm ds}$) for NMOS transistors under seven different gate voltages. (b) Drain current ($I_{\rm ds}$) versus grain voltage ($V_{\rm ds}$) for PMOS transistors under seven different gate voltages.

is basically a polysilicon resistor. The smallest heating unit investigated is 3 μm long and 3 μm wide, considering the current density limitation of the polysilicon resistors.

Electrothermal simulation in a multiphysics FEM tool, COMSOL [22], has been used to optimize the microheater design. The simulation result is shown in Fig. 3(b) and (c), where a polysilicon sheet resistance of 30 $\Omega/\square$ is assumed and all other material properties are chosen according to the employed foundry process [21]. For the simulation, the radiation and convection heat losses are neglected. The bottom surface of the substrate is assumed to remain at room temperature. Fig. 3(b) shows the temperature distribution when a 2.5 V actuation voltage is applied to the heater, which shows a good agreement with the growth pattern [see Fig. 3(b), inset]. Fig. 3(c) is a line plot of the temperature along the heater. It clearly shows the ideal condition for CNT-CMOS integration: a very small, localized high-temperature region for CNT synthesis, and a rapid temperature decrease toward the substrate.

Furthermore, several heater designs with different lengths and widths have been investigated to exploit the geometry limitations. The cold wall for CNT landing is designed in two ways. One is a parallel bridge to form a uniform *E*-field, and the other is a sharp tip to form a converged *E*-field, as shown in Fig. 3(d) and (e), respectively. The gap between the two polysilicon bridges is typically 3–6 μm in order to obtain the proper *E*-field and facilitate the CNT landing.

V. Fabricated Devices and Test Results

Optical microscope images of a CMOS chip before and after post-CMOS processing are shown in Fig. 4(a) and (b), respectively. The total chip area is 1.5 mm × 1.5 mm, including test circuits and 13 embedded microheaters. SEMs of two microheaters are shown in Fig. 4(d) and (e), with resistances of 97 and 117 Ω, respectively. At about 2.5 V, red glowing was observed for the design in Fig. 4(e). This voltage was also used for the CNT growth.

Fig. 5 shows SEM images of a device with successful CNT growth, where individual suspended carbon nanotubes were grown from the 3 μm × 3 μm microheater shown in Fig. 4(e) and landed on the near polysilicon tip. The overall resistance of the CNTs was measured between the microheater and the cold polysilicon wall at room temperature and at atmosphere, as shown in Fig. 6. The typical resistances of *in situ* synthesized CNTs were in the range of several megaohm. This resistance value measured is mainly due to the contact resistance between the CNTs and polysilicon. The native oxide on the microheater surface or the alumina particles in the catalyst might be some of the reasons for the high contact resistance and future investigations are required to characterize the electrical properties of this contact in detail. Use of a different type of catalyst or low temperature annealing after nanotube growth could improve the contact resistance.

After successful synthesis of carbon nanotubes, we also evaluated the influence of the localized heating on nearby CMOS circuits. The spacings between the microheaters and circuits vary from 36 to 60 μm, respectively. Simple circuits, such as inverters, were tested and it was verified that they were working properly after CNT growth. More accurate electrical characterizations were performed at the transistor level. The drain current versus drain-source voltage ($I_{\rm ds}$–$V_{\rm ds}$) was measured for both NMOS and PMOS transistors before and after CNT synthesis using a Keithley 4200 semiconductor characterization system. Fig. 7 shows the dc electrical characteristics of individual transistors showing no considerable change after CNT growth, demonstrating the CMOS compatibility of this integration approach.

VI. Conclusion

In conclusion, a monolithic CNT-CMOS integration approach has been proposed and experimentally verified. This approach utilizes localized heating to simultaneously achieve high temperature required for CNT growth and low temperature for CMOS circuit protection on the same chip. The fabrication is based on maskless post-CMOS processing. CNT-CMOS interconnect is realized without the need of any photolithography or metal deposition. The fabrication is fully compatible with commercial CMOS foundry processes. CNTs have been successfully grown on specific locations determined by local

temperature and electric field distributions, without deteriorating neighboring CMOS circuits. This simple, low-cost and scalable integration method is promising for making various nanodevices and integrated micro/nanosystems.

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